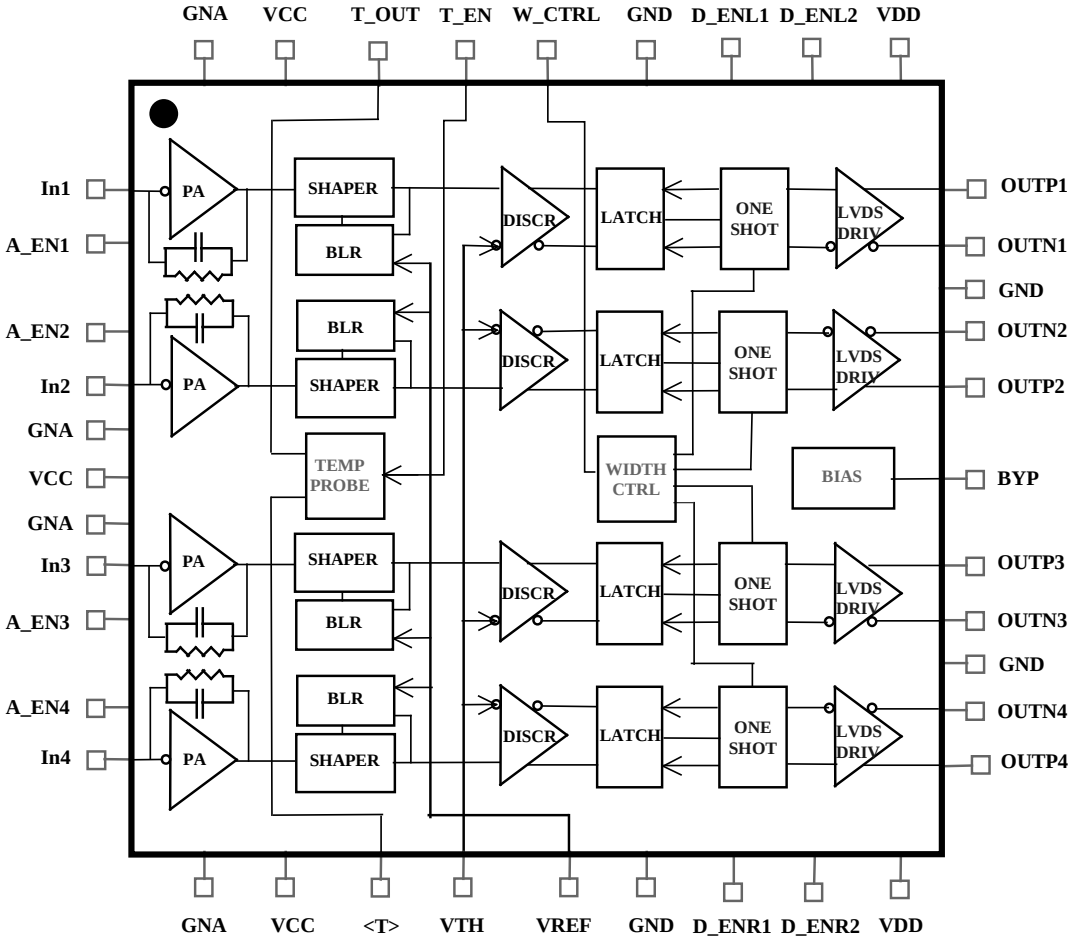
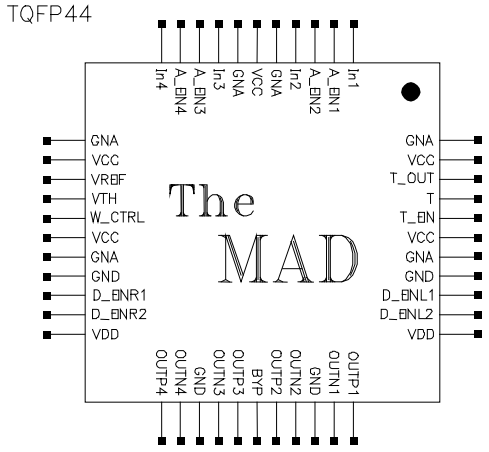
MAD FE ASIC

A short description

The integrated circuit has been designed using BYE technology (BiCMOS 0.8 μm) as from HIT-KIT v3.10. Die area is 2.5x2.5mm^2 and it has to be housed in TQFP44 package.

One chip contains four independent analog chains. Two separate power supplies are foreseen, in order to minimize mutual interference, for the input section (Vcc=5V) and for the output stages (Vdd=2.5V); several pins are reserved for power and for ground that is as well different for the input (GNA) and for the output (GND). The block diagram and pinouts of the chip is shown here below, the table in the next page lists all pins and their use.





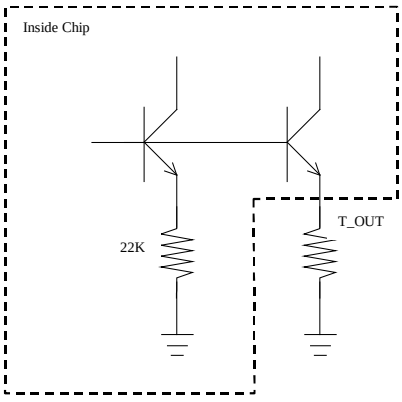
PIN	Meaning	An./Digi	In/Out	Notes
GNA	Analog ground	-	-	-
GND	Digital ground	-	-	-
VCC	+5V power supply	-	-	Capacitor of 100nF to ground
VDD	+2.5V power supply	-	-	Capacitor of 100nF to ground
BYP	Internal reference voltage output	A	O	Capacitor of 100nF to ground
VTH	Threshold voltage	A	I	VREF + threshold (3mV/fC)
VREF	Signal reference baseline voltage	A	I	Usually 1.5V
In(1-4)	4 input channels	A	I	-
T_OUT	Temperature probe output, externally enabled with pin T_EN	A	O	About 7.5mV/°K, low Z out 22KΩ resistor to ground
<T>	Temperature probe output	A	O	About 7.5mV/°K, high Z out
T_EN	T_OUT enable (logic level high, internally pull up)	D	I	TTL level
A_EN(1-4)	4 analog masks enable (logic level high, internally pull down)	D	I	TTL level
D_ENR(1,2)	Digital right mask enable (D_ENR1 high, D_ENR2 low)	A	I	High: 1.5-1.6 V Low: 1.2-1.3 V
D_ENL(1,2)	Digital left mask enable (D_ENL1 high, D_ENL2 low)	A	I	High: 1.5-1.6 V Low: 1.2-1.3 V
W_CTRL	Control of output width, common to all channels	A	I	Usually resistor to ground
OUTN1, OUTP1	Differential output channel 1, LVDS compatible levels	A	O	120Ω terminating resistor between
OUTN2, OUTP2	Differential output channel 2, LVDS compatible levels	A	O	120Ω terminating resistor between
OUTN3, OUTP3	Differential output channel 3, LVDS compatible levels	A	O	120Ω terminating resistor between
OUTN4, OUTP4	Differential output channel 4, LVDS compatible levels	A	O	120Ω terminating resistor between

Each channel is made of a low noise charge preamplifier followed by a shaper whose quiescent level is set by a baseline restorer to an external reference voltage (pin VREF) common to the four chains. A negative charge pulse applied to the input of the preamplifier causes a positive signal at the output of the shaper, superimposed to the reference level, that is compared against an external threshold (pin VTH), common to the four channels, by a fast discriminator; its output is stretched by a latch enabled by a one-shot, whose pulse width is inversely proportional to the current sunk from W_CTRL pin, again shared by all channels.

The non retriggerable pulse so produced is then buffered by a differential voltage driver and the outputs (pins OUTP(1-4) & OUTN(1-4)) are able to feed a 120Ω load placed across them with LVDS compatible levels.

Each channel can be disabled by a TTL high level applied to pins A_EN(1-4), recovery to normal operation requires about 10μs. Channels 1 & 2 (left channels) can be enabled/disabled in about 30ns by a differential signal applied to pins D_ENL(1-2), the same for right channels 3 & 4 via pins D_ENR(1-2).

An absolute temperature sensor is included in the chip, having an output of 7.5mV/°K that is available at pin <T> and at pin T_OUT (22kΩ external resistor to ground) after a unity gain buffer enabled by a TTL high level applied to pin T_EN.

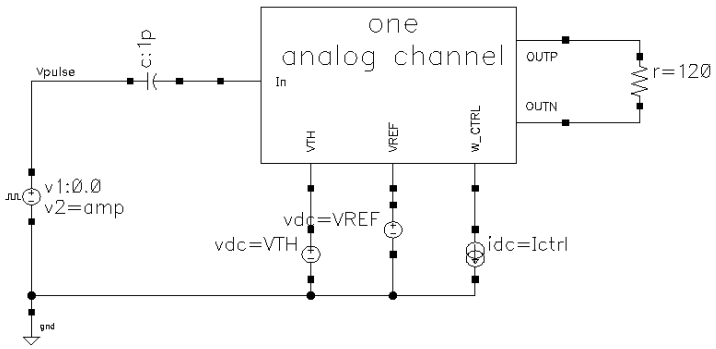


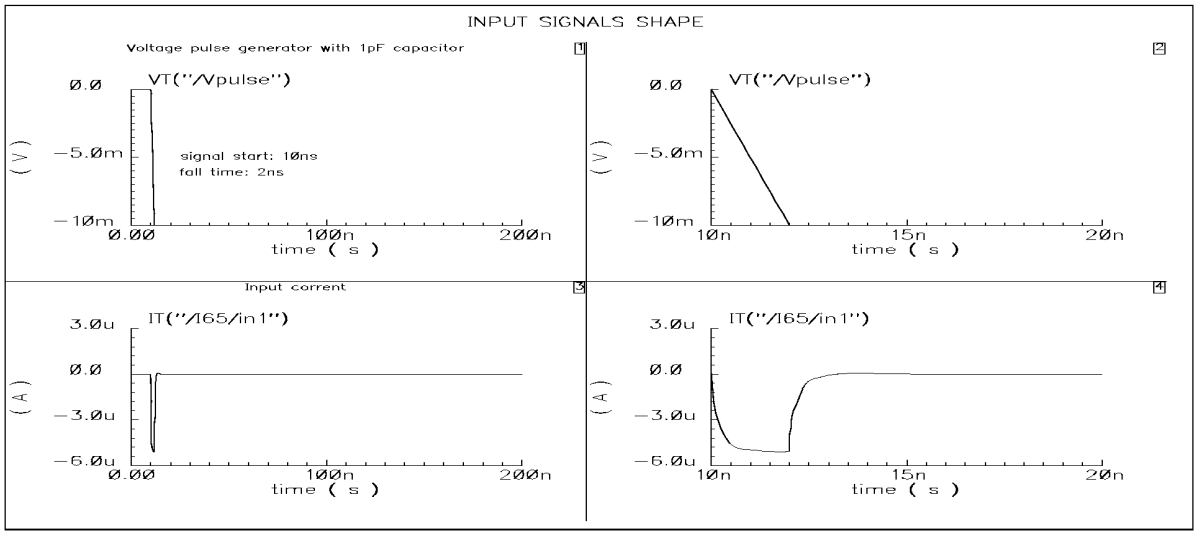
An internal generator biases the whole chip, its output is connected to pin BYP for bypassing with a capacitor to GNA.

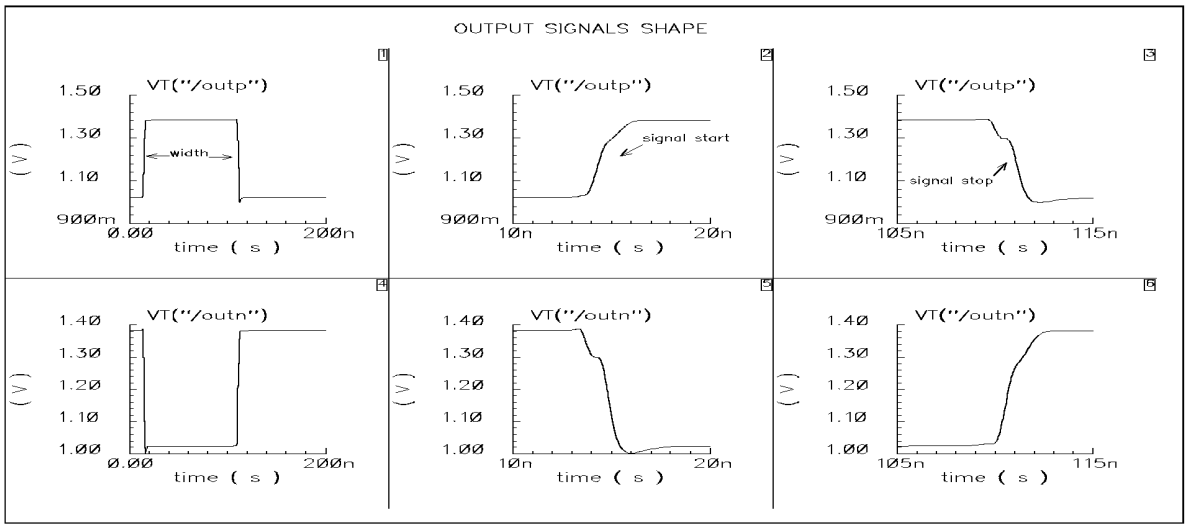
Input and output signals description

The figures in this page present the simulated behavior of one electronic chain of the ASIC excited by a voltage pulse generator. In this simulation the pulse generator is started at 10ns from time origin with amplitude of 10mV (note that we are interested in negative charges, so the trigger time has to be taken at the falling edge of the generator pulse).

The figures show the voltage across the generator, the preamplifier input current and the output differential signals across a 120Ω resistor load; the duration of the output signals is set at about 100ns by a current sinking generator of 20µA (the same width can be obtain with a 200KΩ resistor to ground).







Control signals description

The ASIC has some control signals for setting the threshold/reference voltages, enabling digital and analog masks and the temperature probe output:

- 2 control voltages for threshold and baseline reference:
  - VREF: shaper output baseline voltage, range from 1 to 3 V and usually set at 1.5V
  - VTH: discriminator threshold voltage, VREF plus threshold value (about 3mV/fC)
- 1 digital control input for enabling temperature probe output T_OUT (internally pull up), T_EN:
  - T_OUT enable: TTL level high
  - T_OUT disable: TTL level low
- 4 digital control inputs for analog masks (internally pull down), A_EN(1-4):
  - mask enable (channel disable): TTL level high
  - mask disable (channel enable): TTL level low
- 2 differential control inputs for digital masks, D_ENR(1,2) and D_ENL(1,2):
  - mask enable (channel disable): D_EN(R/L)1 high, D_EN(R/L)2 low
  - mask disable (channel enable): D_EN(R/L)1 low, D_EN(R/L)2 high

The figures below show the characteristics of the control signals for masks and temperature probe features. Note that even if high levels of analog mask and temperature probe are set to 5V, actually only a TTL compatibility is required.