A PROTOTYPE FRONTEND ASIC FOR THE MUON CHAMBERS OF CMS BARREL

F.Gonella and **M.Pegoraro**

ISTITUTO NAZIONALE DI FISICA NUCLEARE

Sezione di Padova

REMARKS

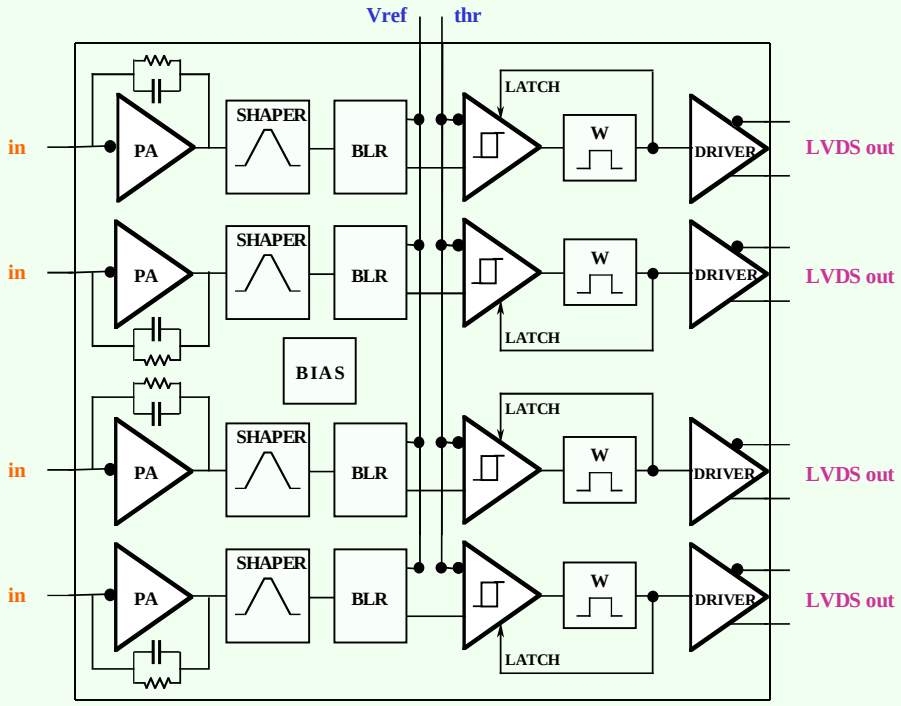
- **Gas mixture Ar CO_2 85:15 @ atmospheric pressure**
- **Drift rate 50 μm/ns; max drift time 400 ns**
- **Low gain (50 K - 100 K) for long lifetime**

➨ **Main goals are efficiency & time resolution**

- The frontend task is to amplify signals, discriminate them against an external threshold and transmit the results to data acquisition.
- Input impedance as close as possible to that of detector.
- Low noise, high gain analog chain.
- Fast rise time to minimize time walk due to different amplitude signals from drift tubes.
- Low offset both for the shaper output and the discriminator input.
- Built in hysteresis for speed and stability.
- Adjustable output width to override cable bandwidth.
- Fast, low level (LVDS) cable driver to minimize power and interferences.
- Finally these tasks must be accomplished in the smallest space and consuming very little power in order to reduce service costs and maximize active volume.

CHIP PRESENTLY UNDER TEST

Block diagram & main features



CHARACTERISTICS

0.8 µm BiCMOS technology

4 complete channels in 2.5 x 2.3 mm^2 die area

28 pin CLCC J-type package

25 mW/channel @ + 5 V & + 2.5 V

noise ~ 1500 ē ; slope ~ 100 ē /pF

sensitivity ~ 3.3 mV/fC ± 10% max tolerance

Zin ~ 200Ω (5 MHz - 200 MHz)

max input before saturation ~ 800 fC

threshold range 0 - 600 fC with ± 0.5 fC accuracy (+ gain accuracy)

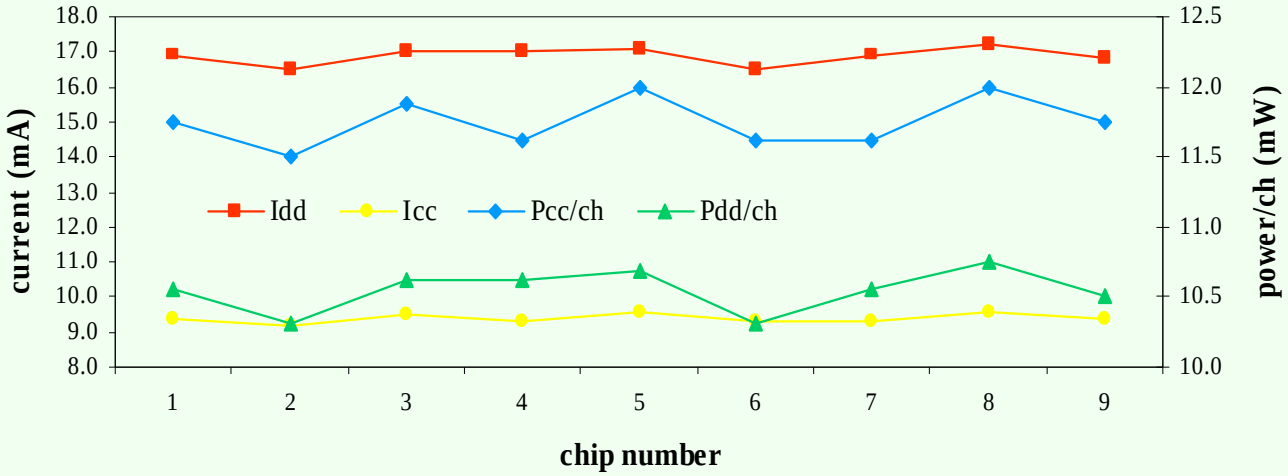
max input rate without loss of accuracy > 2 MHz @ 1 pC

one shot width 20 - 200 ns

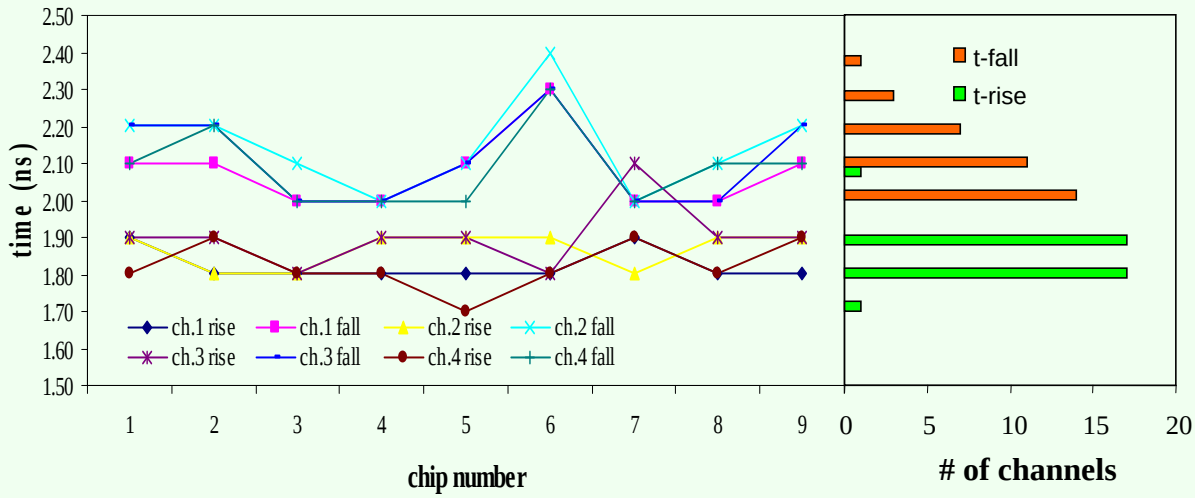
LVDS compatible cable driver

GENERAL TESTS
Power & output

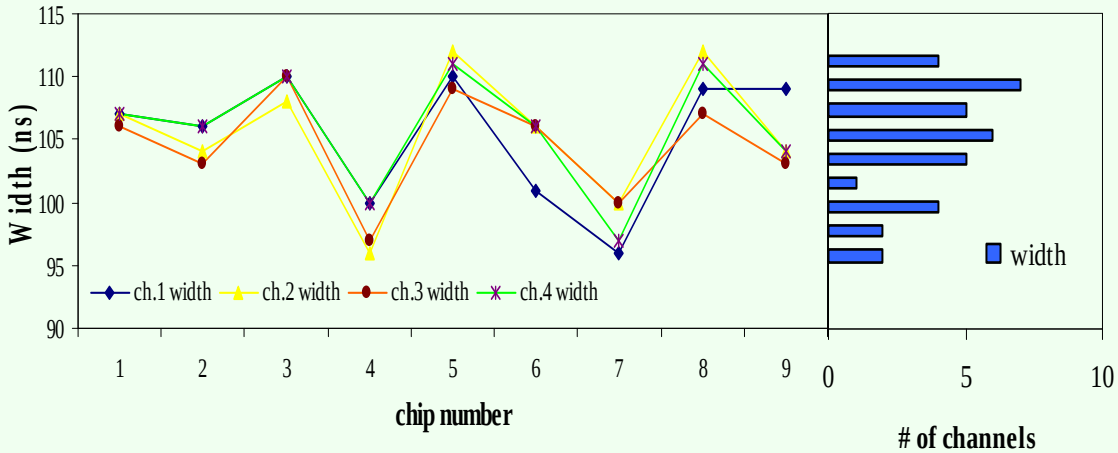
Current drawn (Vcc,Vdd) & power dissipation



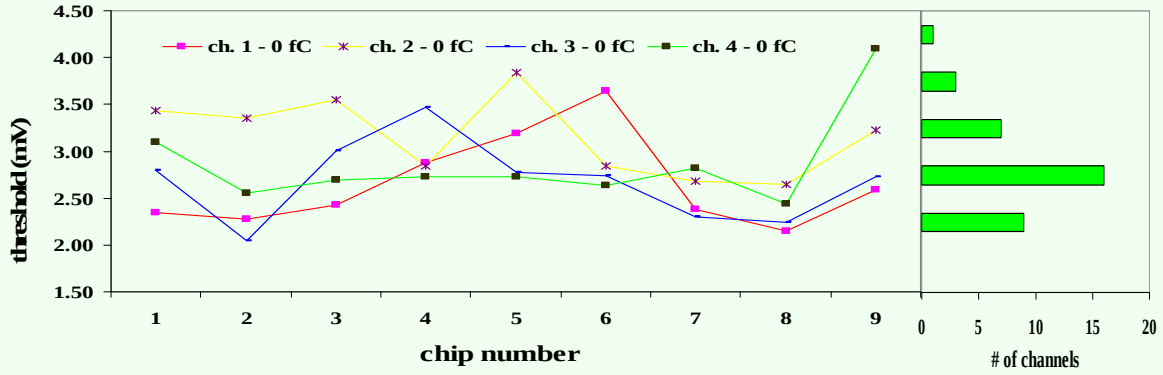
Rise & fall time



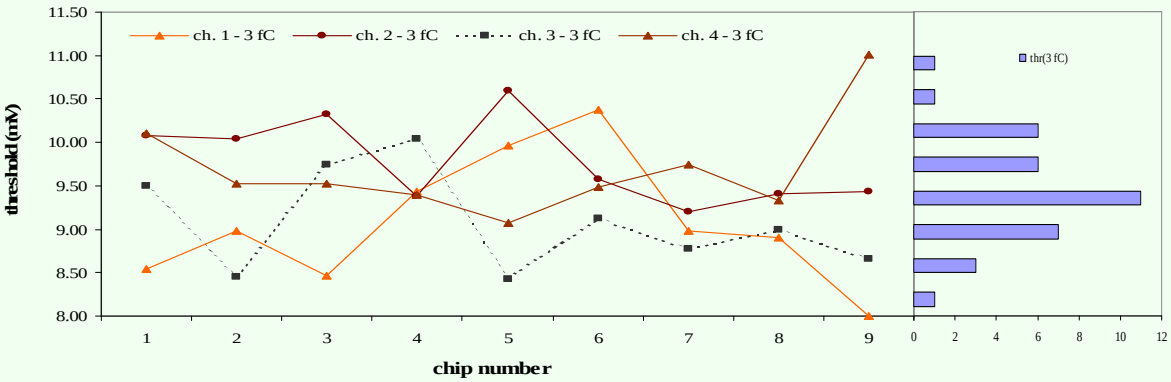
One shot pulse width



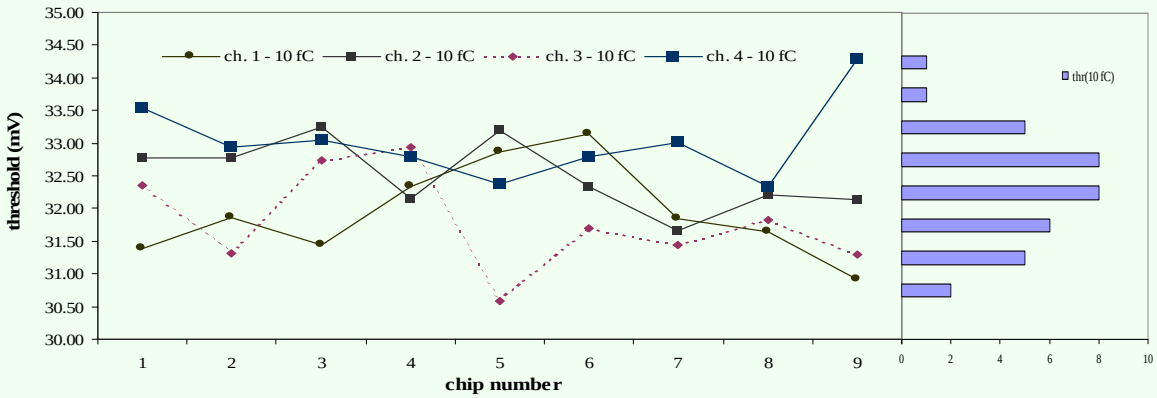
GENERAL TESTS
Threshold uniformity



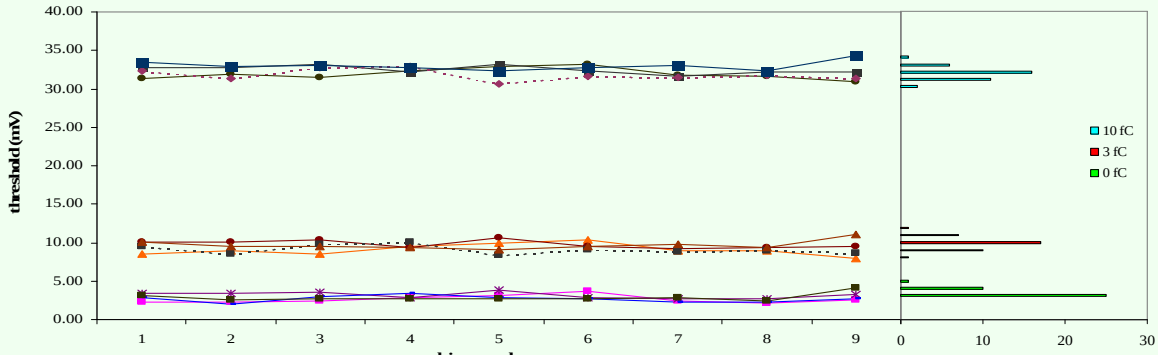
Threshold distribution @ 3fC input



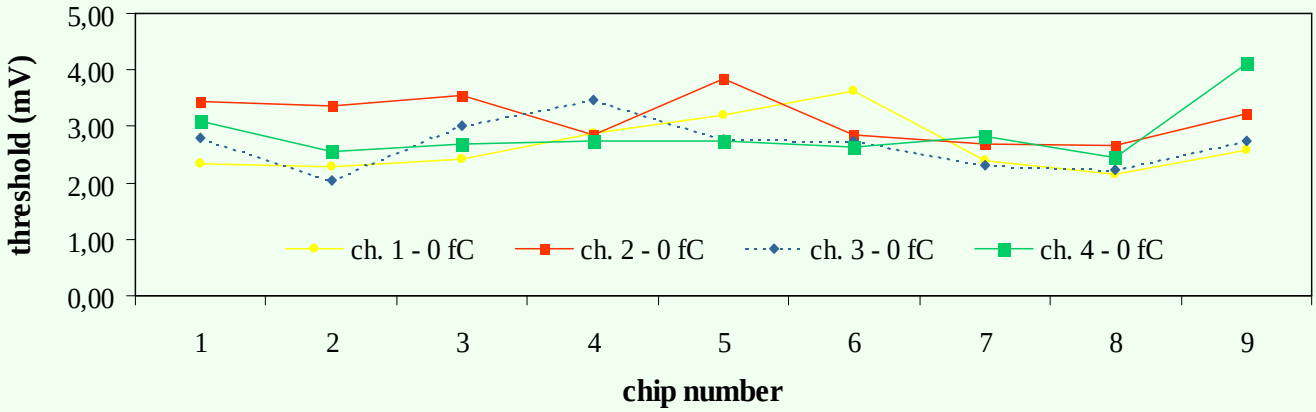
Threshold distribution @ 10fC input



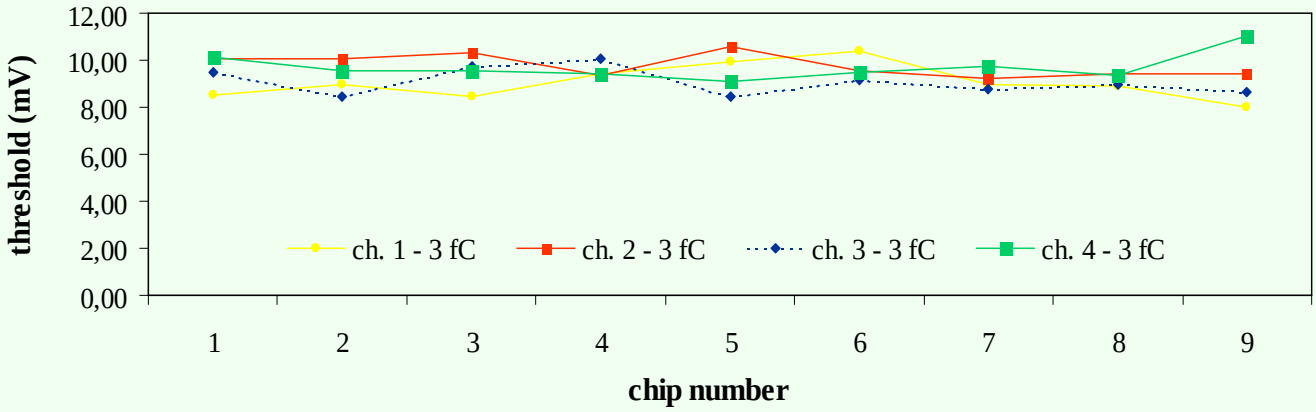
Summary of threshold @ 0, 3 & 10 fC



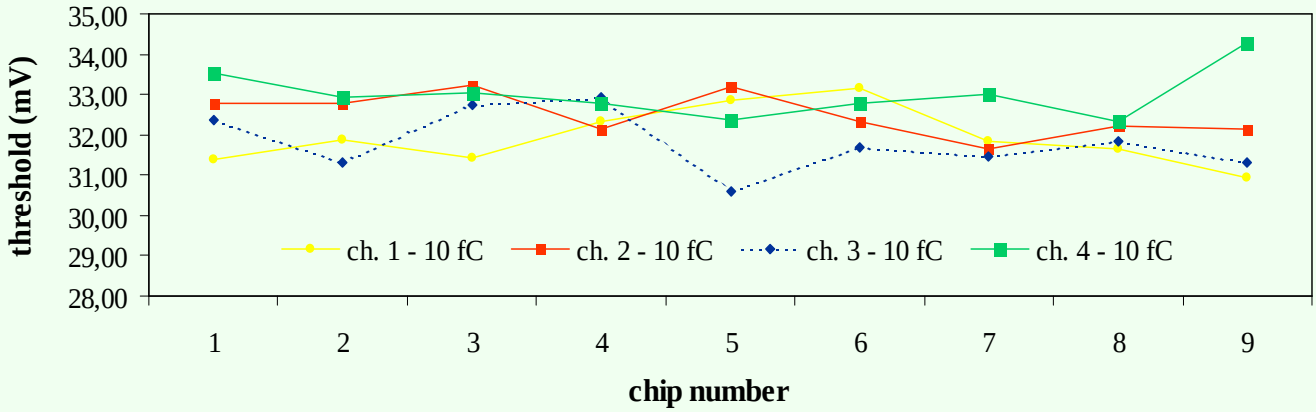
Threshold distribution @ 0 fC



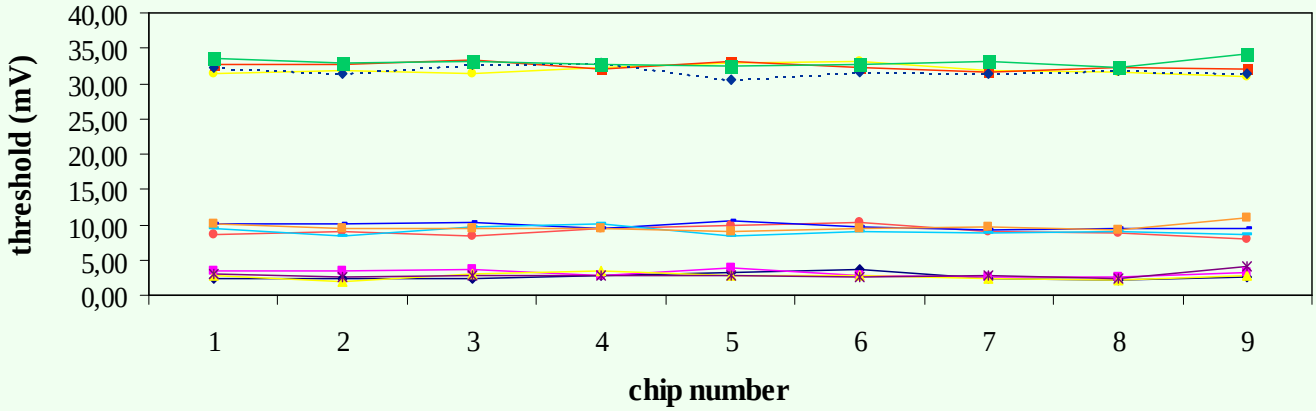
Threshold distribution @ 3fC input



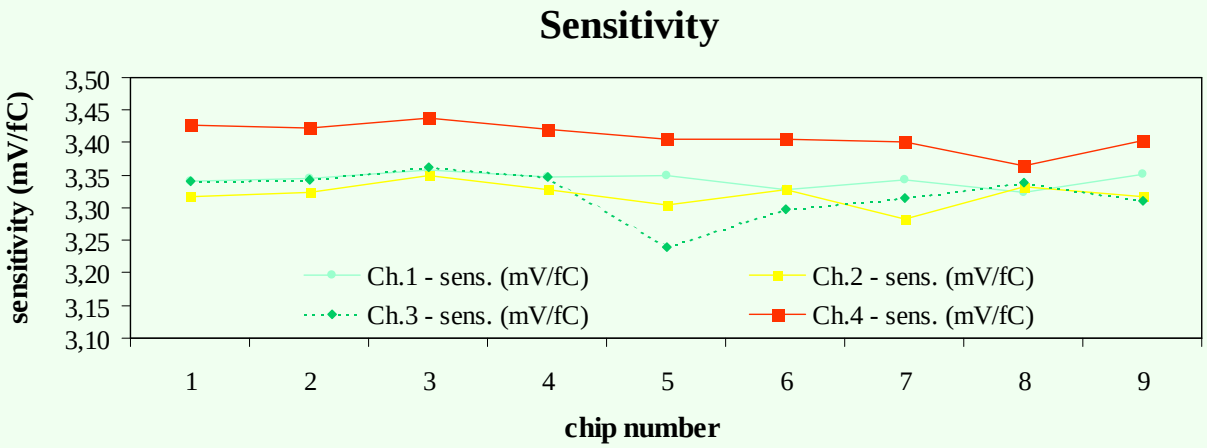
Threshold distribution @ 10fC input

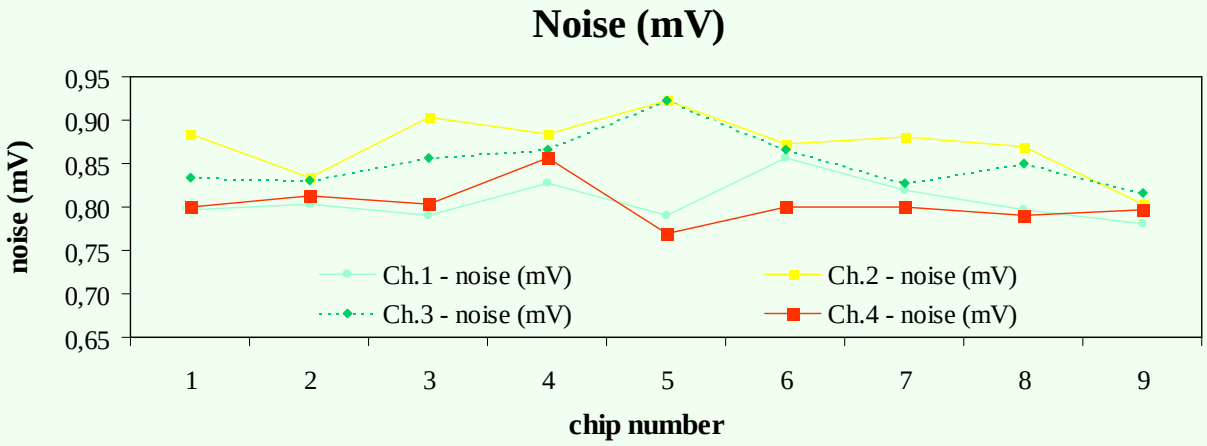


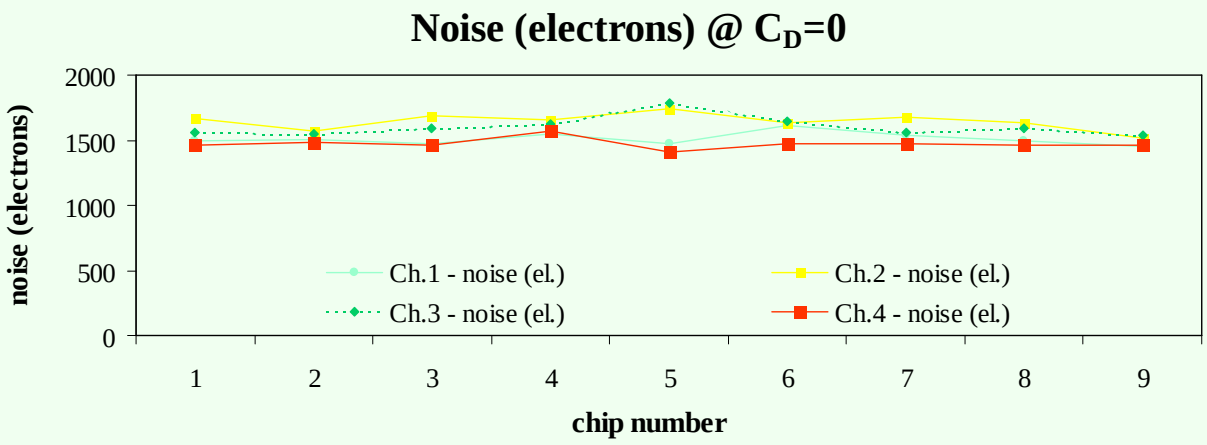
Summary of threshold @ 0, 3 & 10 fC



GENERAL TESTS
Sensitivity & Noise

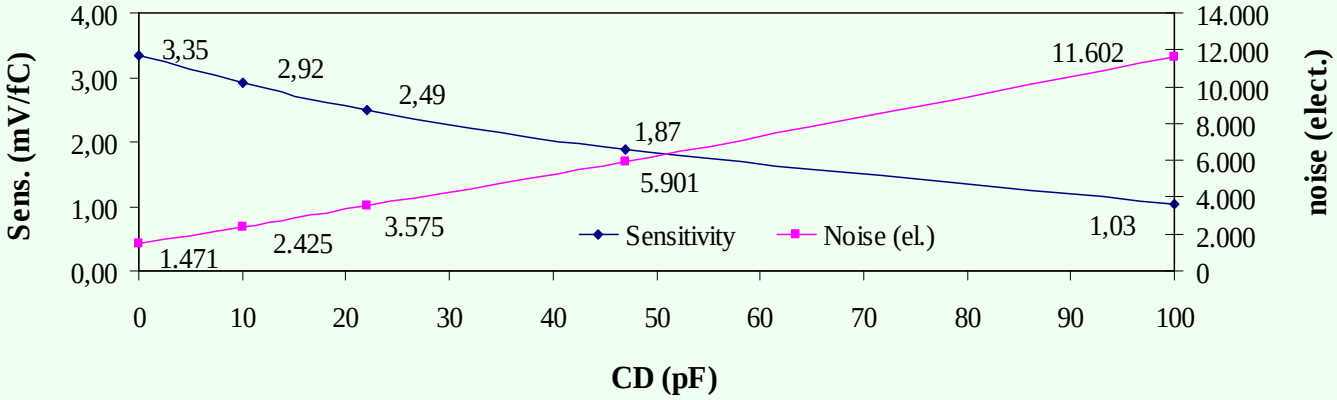




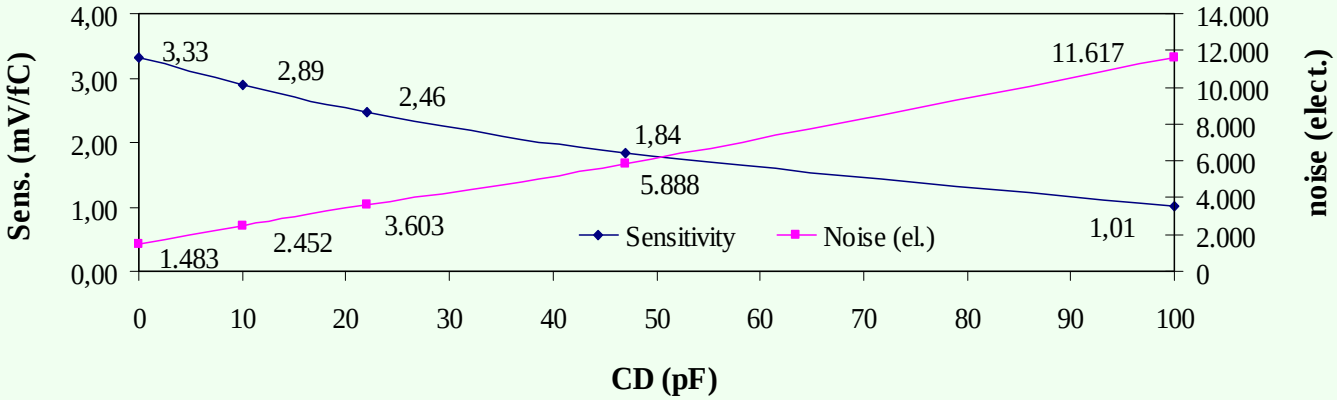


GENERAL TESTS
Noise vs. C_D

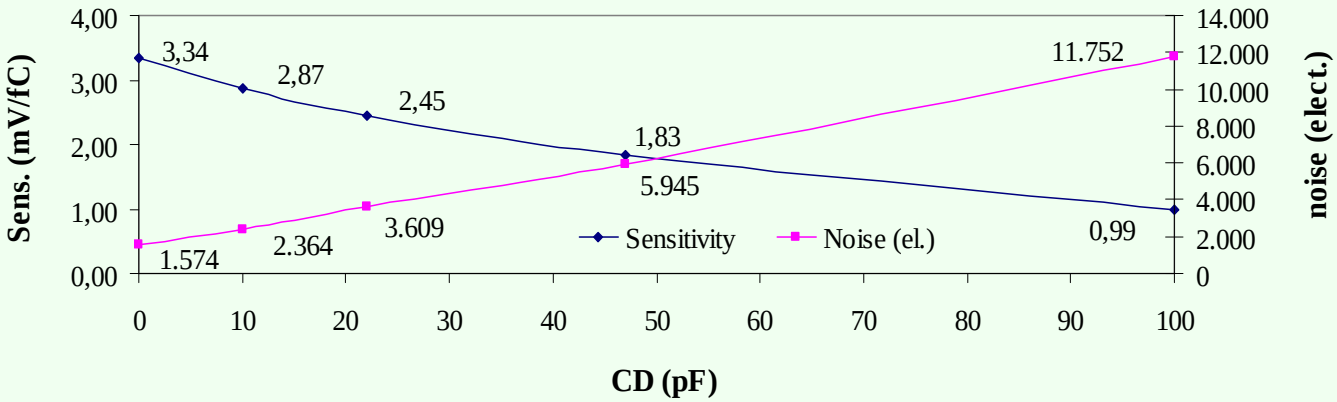
Noise & sensitivity vs. CD (chip 5)



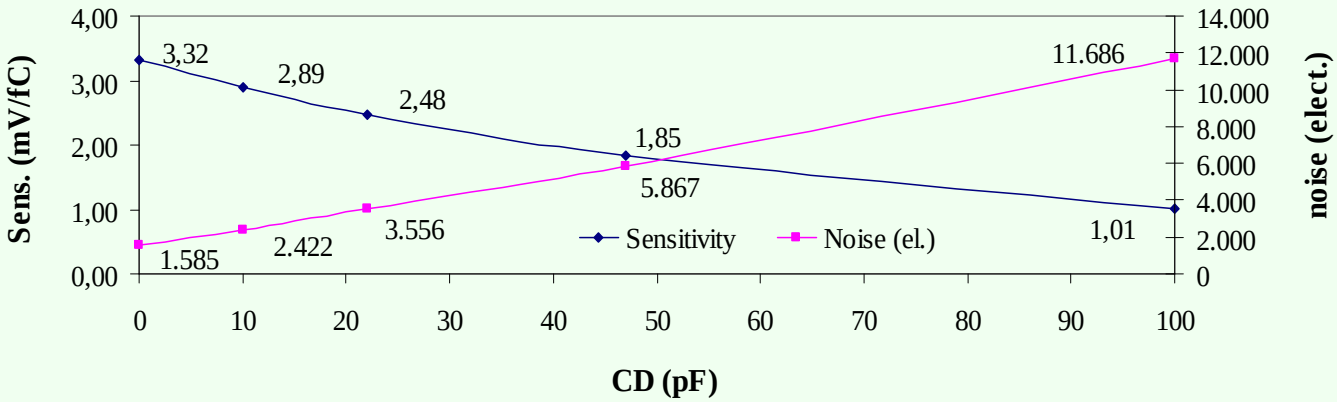
Noise & sensitivity vs. CD (chip 6)



Noise & sensitivity vs. CD (chip 7)

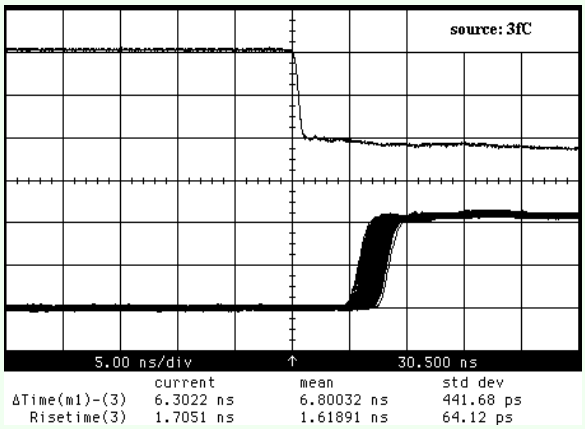


Noise & sensitivity vs. CD (chip 8)

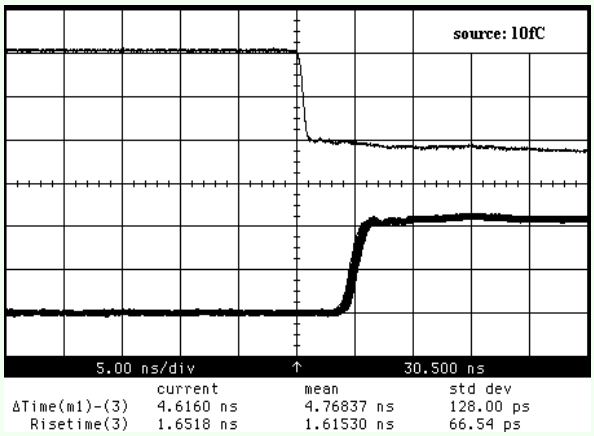


GENERAL TESTS
Time walk 1

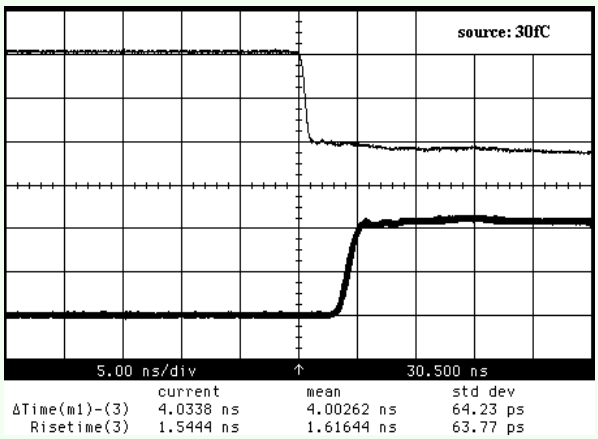
Fixed threshold : 1.5 fC. Different input charges



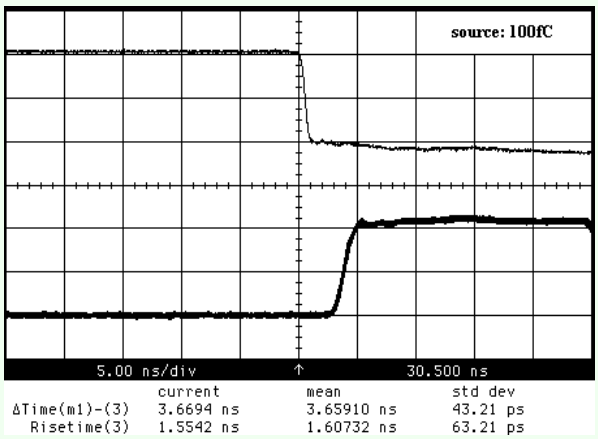
Input = 3 fC delay = 6.8 ns



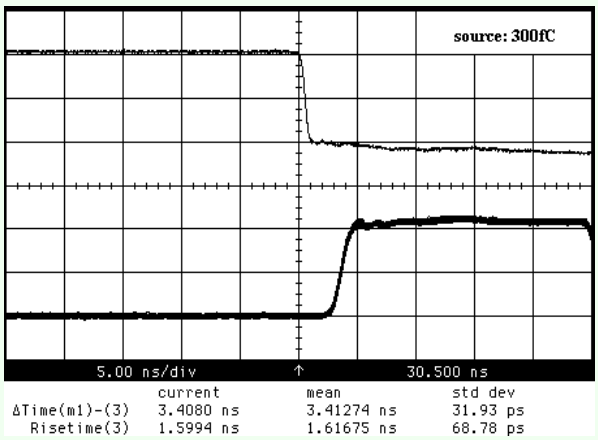
Input = 10 fC delay = 4.8 ns



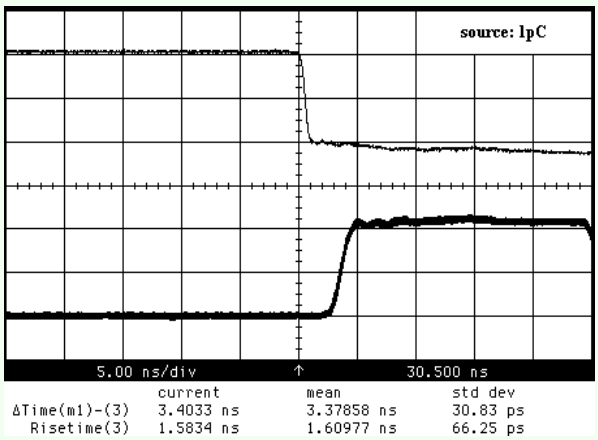
Input = 30 fC delay = 4.0 ns



Input = 100 fC delay = 3.7 ns



Input = 0.3 pC delay = 3.4 ns



Input = 1.0 pC delay = 3.4 ns

GENERAL TESTS
Time walk 2

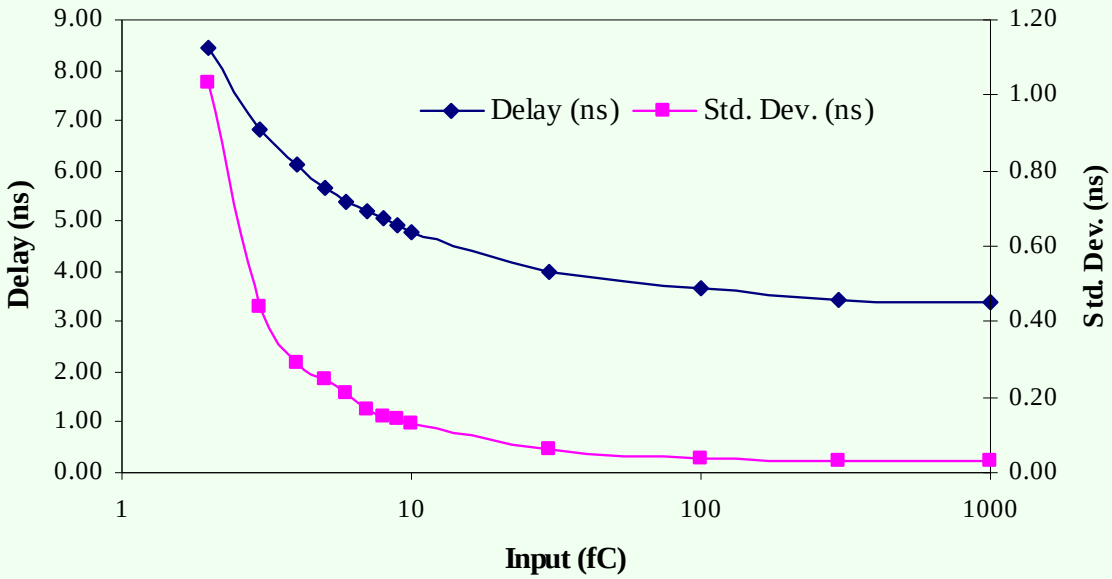
Fixed threshold : 1.5 fC; different input charges
PLOT OF ALL DATA

We are interested in low values of threshold since low detector gain requires to work in the range below 10 fC.
The r.m.s. plot shows the contribution of noise to worsening of time resolution.

CHIP 8 ; ch 2

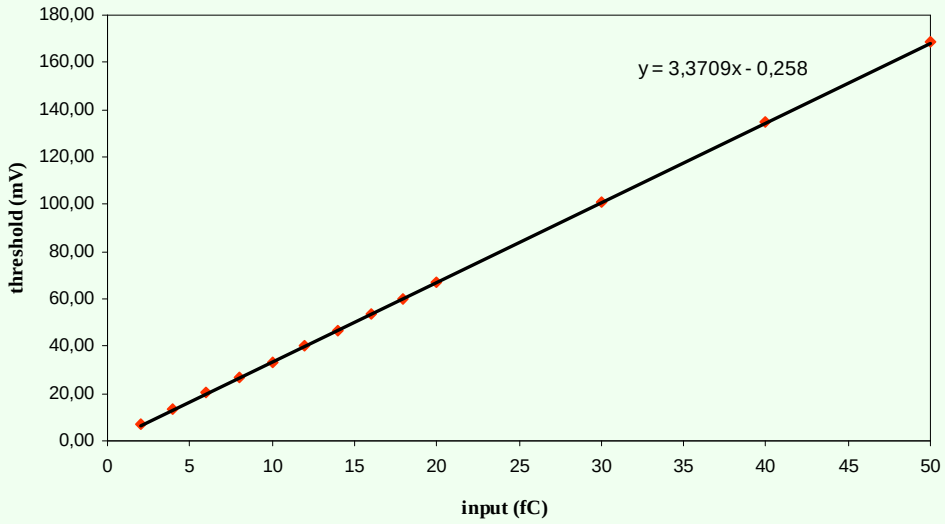
Input (fC)	Delay (ns)	Std. Dev. (ns)
2	8,46	1,03
3	6,80	0,44
4	6,11	0,29
5	5,65	0,25
6	5,39	0,21
7	5,19	0,17
8	5,04	0,15
9	4,91	0,14
10	4,77	0,13
30	4,00	0,06
100	3,66	0,04
300	3,41	0,03
1000	3,38	0,03

Time Walk (chip 8, ch 2)

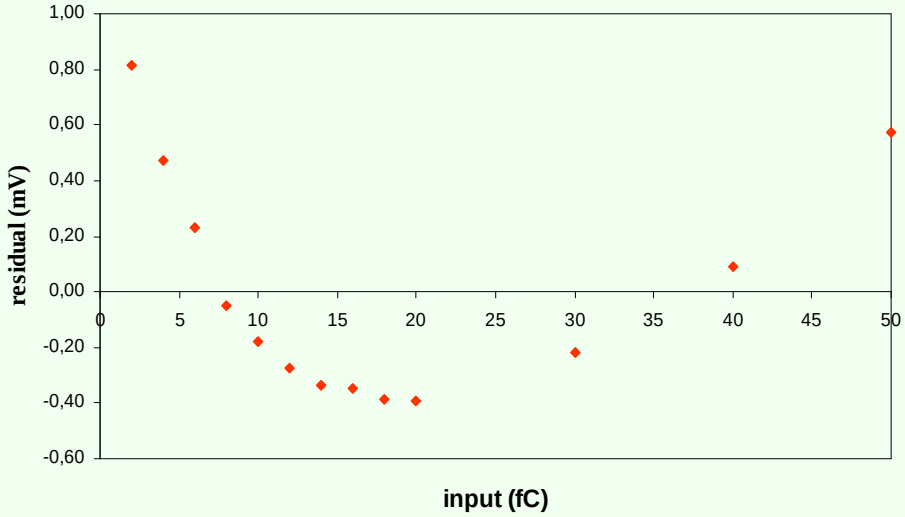


THRESHOLD LINEARITY
Low Threshold

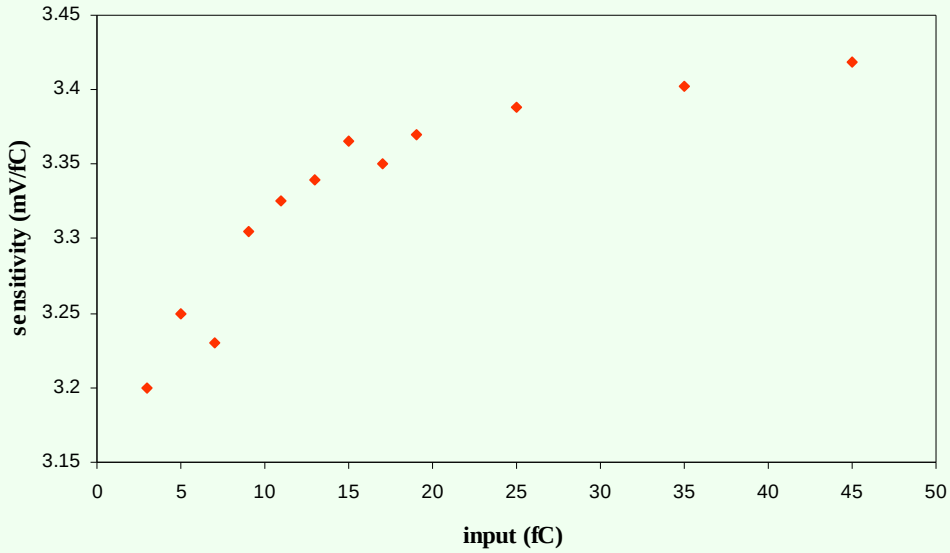
low threshold linearity



Residual

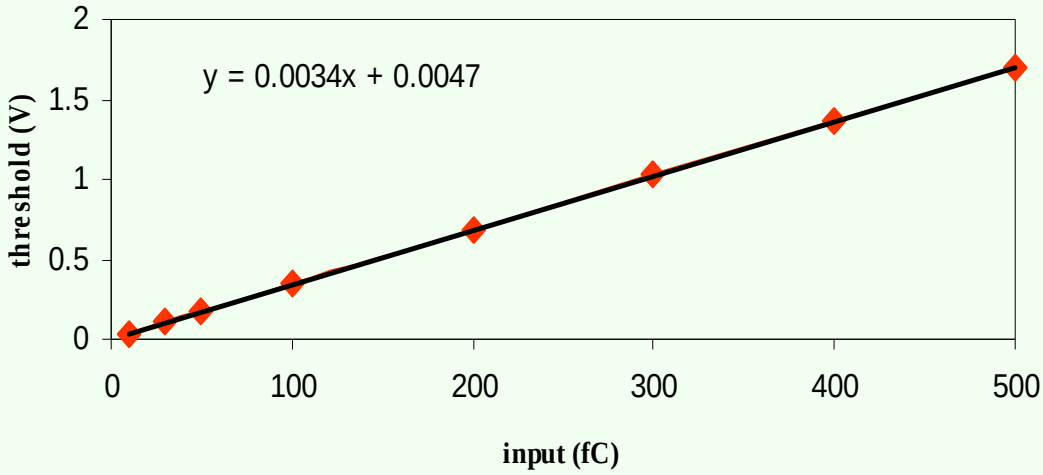


Sensitivity

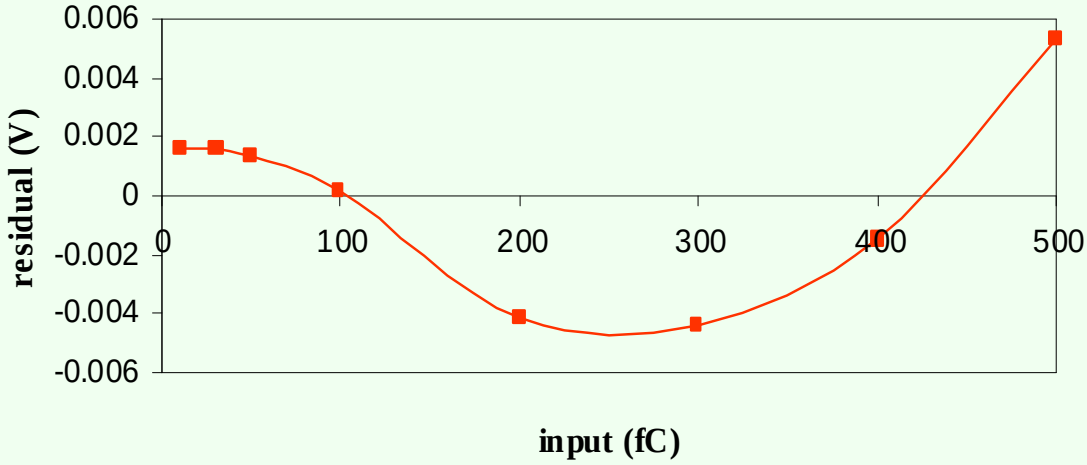


THRESHOLD LINEARITY
High Threshold

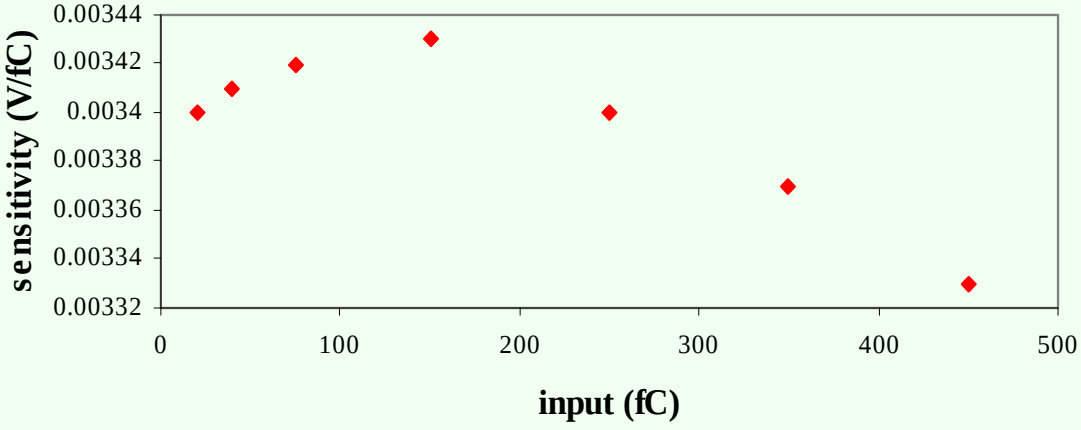
High threshold linearity



Residual

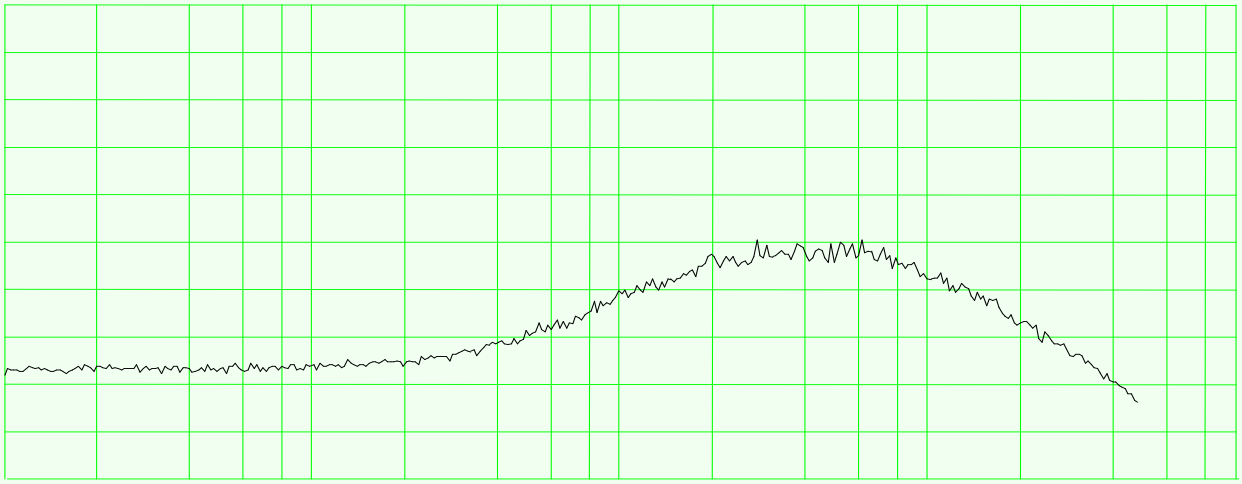


Sensitivity

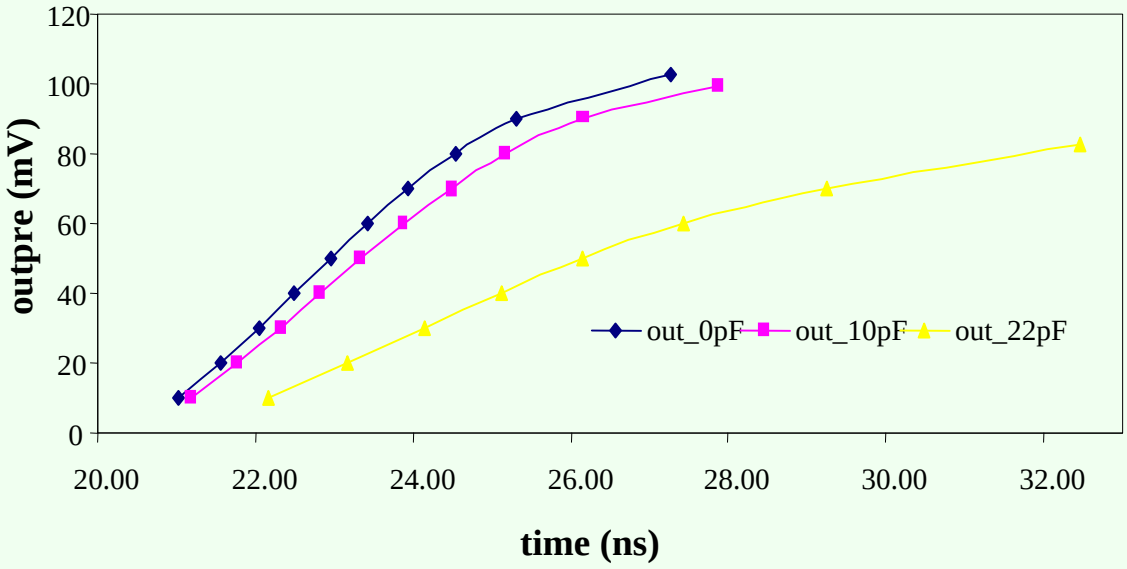


ANALOG TESTS
Zin, rise time & slew rate

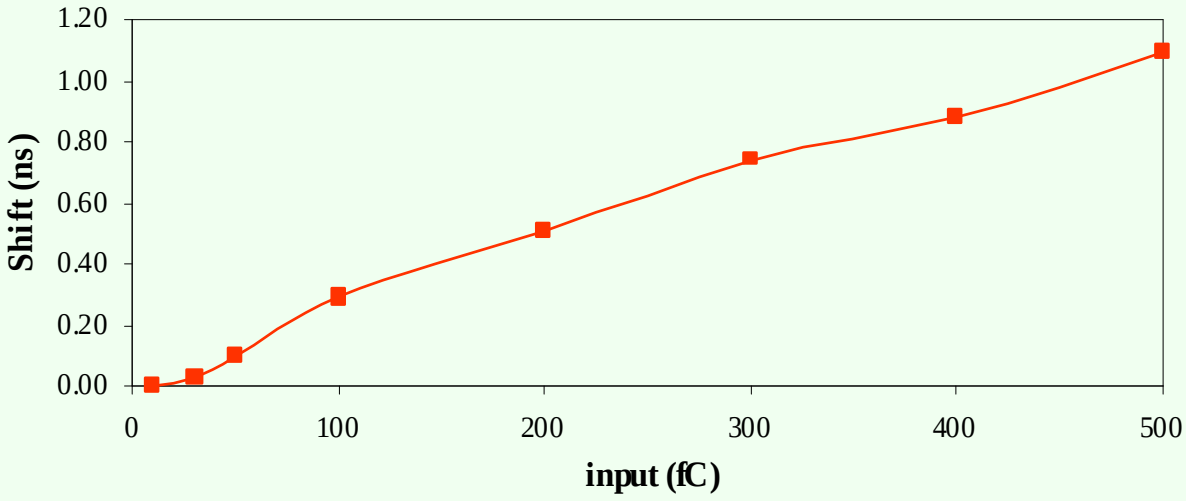
Zin vs. frequency (100 KHz-1GHz; vertical scale 50Ω/div)



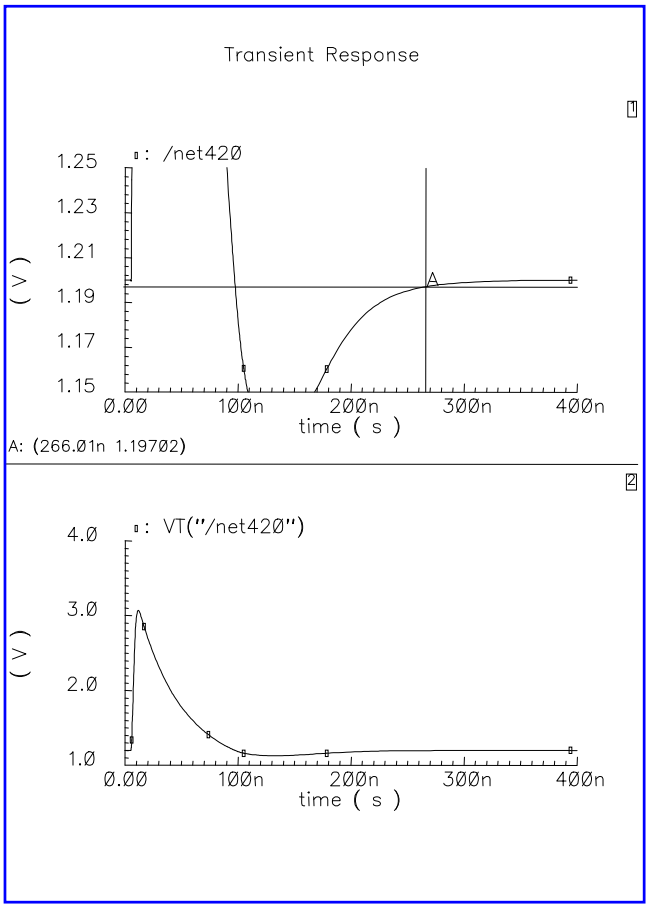
Output shaper (input 30fC)



Peaking Time Shift



ANALOG TESTS
Max signal rate & crosstalk



This is a simulation plot. Actually test was performed by injecting 1 pC pulses with a photodiode @ 2 MHz and delayed 3 fC pulses using a capacitor and pulse generator. Threshold was fixed to detect 50% of generator rate without light pulses.
No difference was noticed with light on when reducing the delay between the two pulses to less than 500 ns.

CROSSTALK

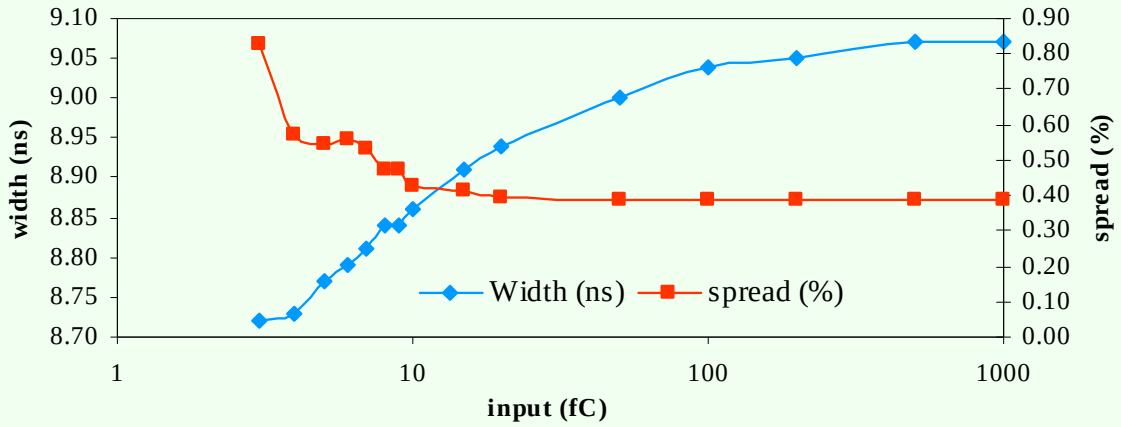
3 different cases have been studied :

a) negative charge inputs 0.3%
b) positive charge inputs .....0.5% (fixed)
c) output drivers to analog input ..... 5fC (fixed)
this is the case of unterminated cables

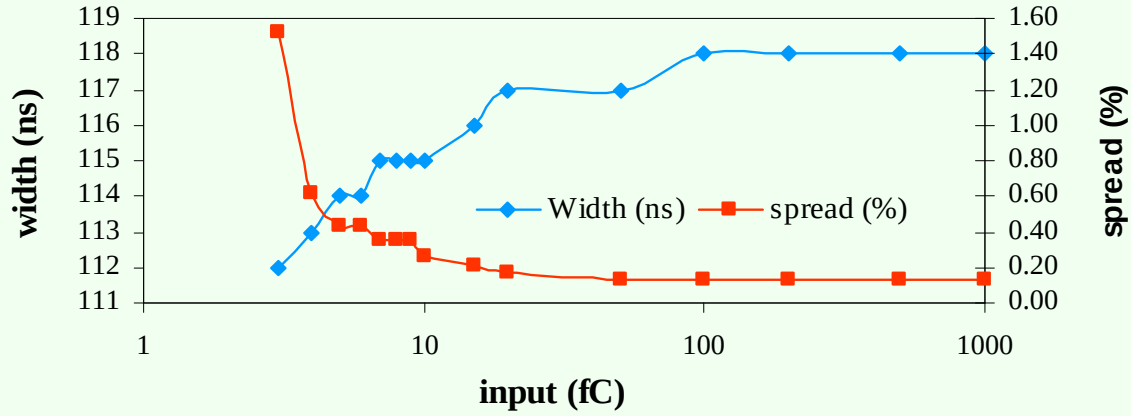
case b) has been reduced to case a) changing the circuit; possible solution implemented in next prototypes that will include all improvements

ONE SHOT WIDTH
Max, min & dependence

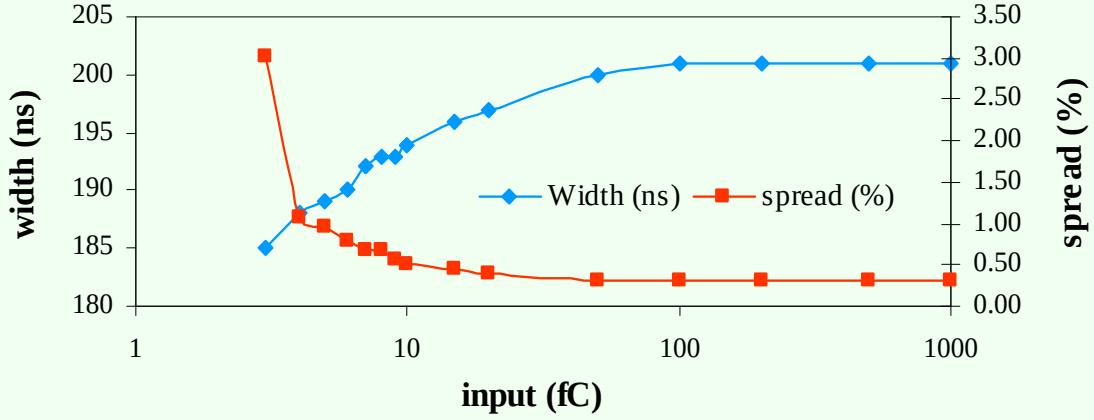
Min width



Typ width

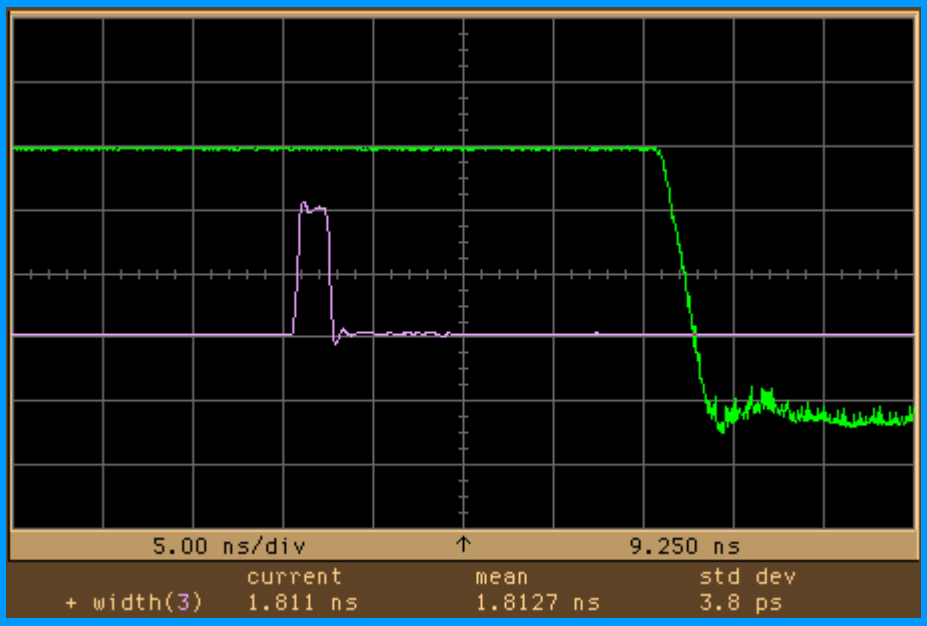


Max width

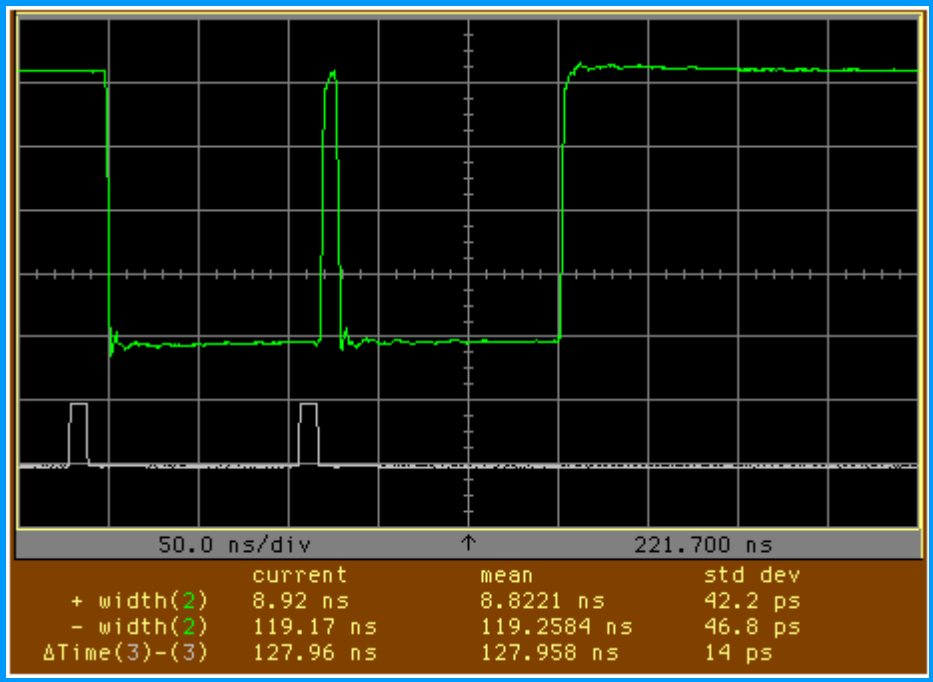


TIMING SIGNALS
Discriminator & one shot

Minimum width of dicriminator input signal
1.8 ns pulses with 5 mV overdrive are captured
with 99.9 % efficiency

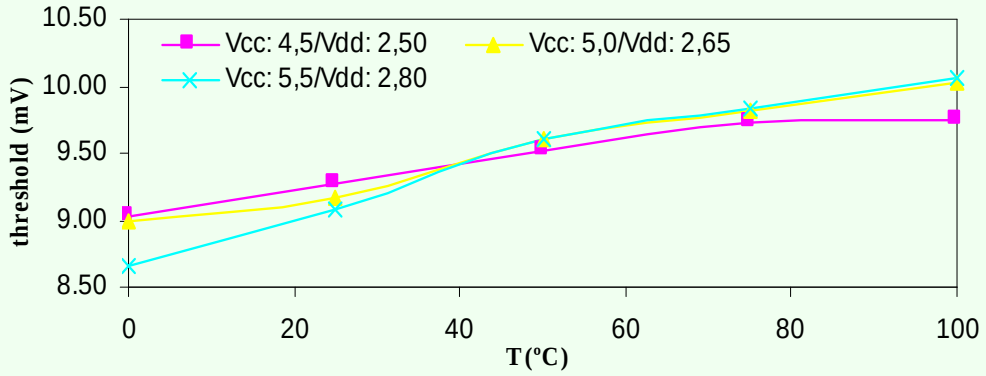


One shot dead time
9 ns @ 100 ns pulse width

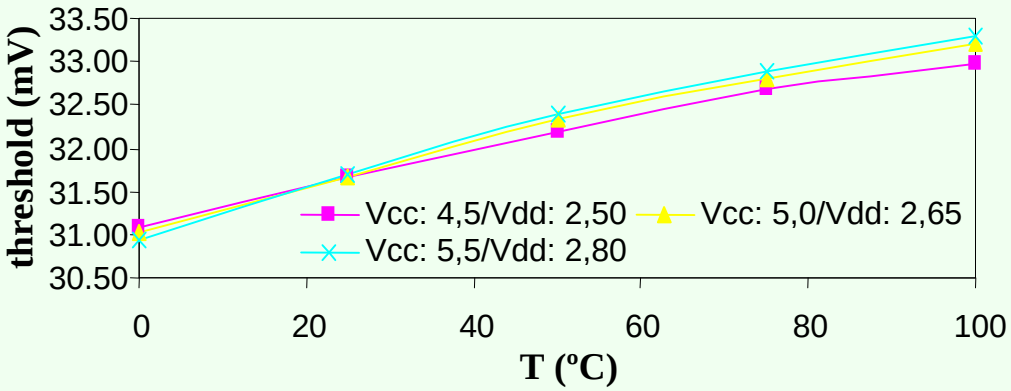


TEMP. & SUPPLY DEPENDENCE
Threshold, noise & sensitivity

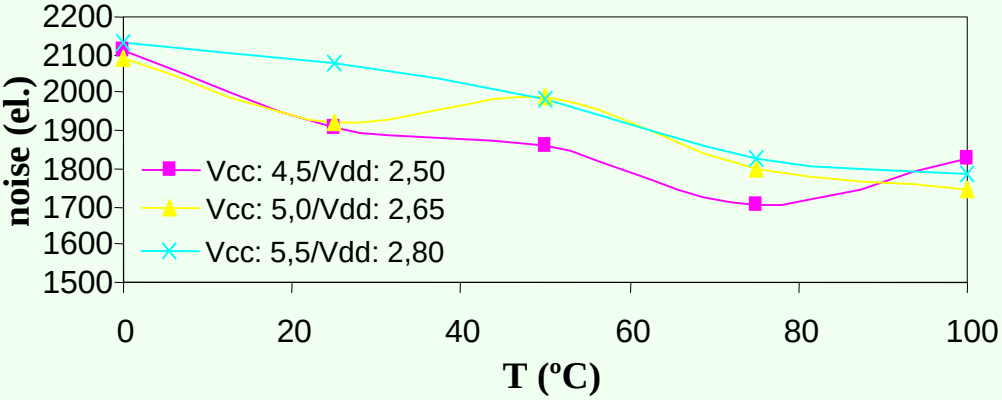
3fC threshold variation



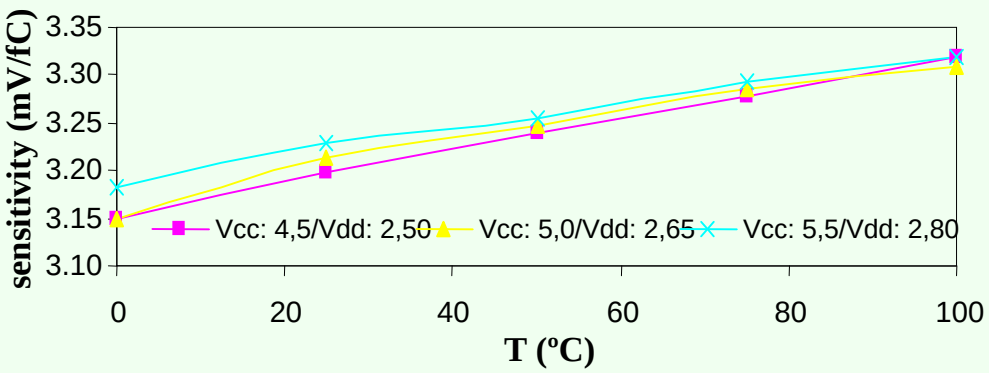
10fC threshold variation



noise



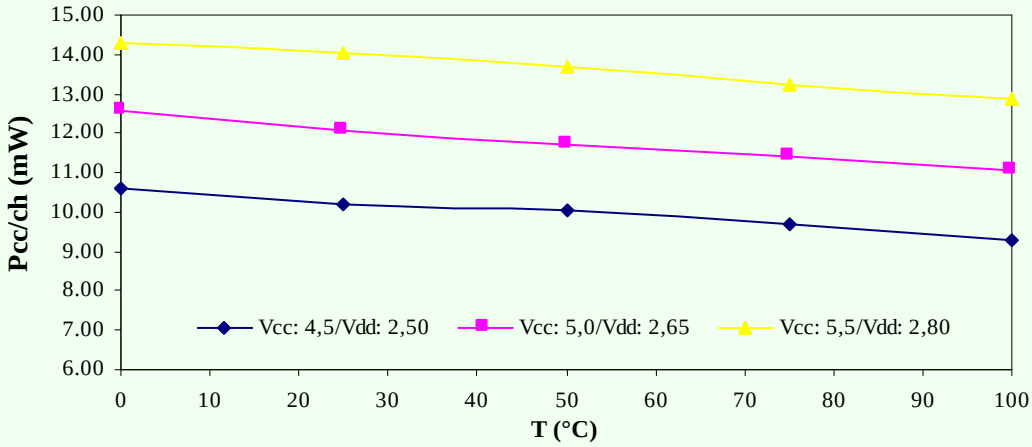
sensitivity



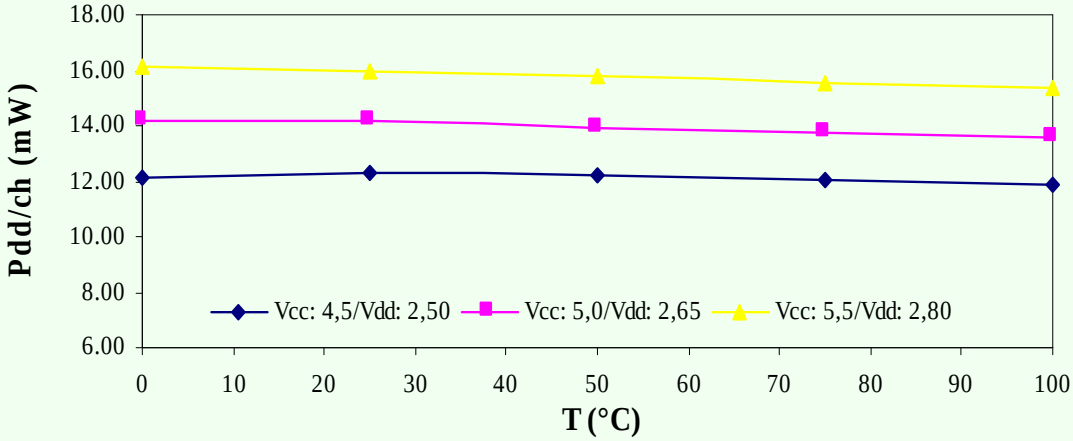
TEMP. & SUPPLY DEPENDENCE

Power dissipation & output levels

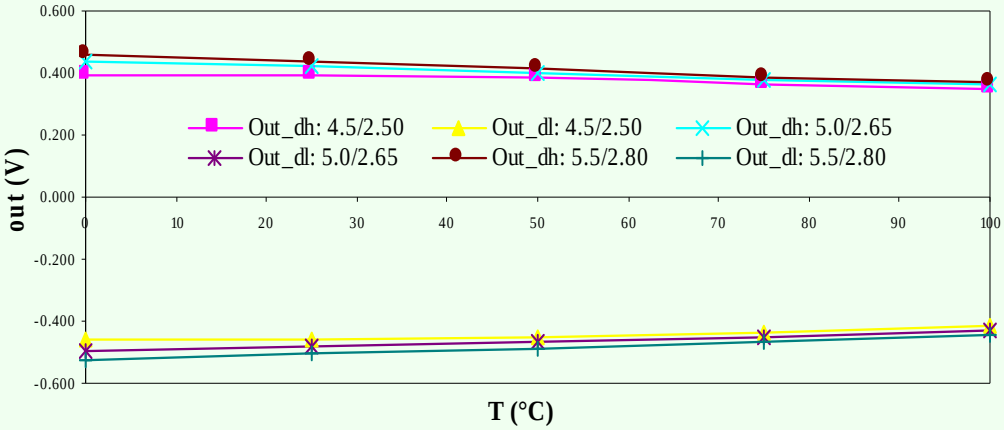
Pcc/channel



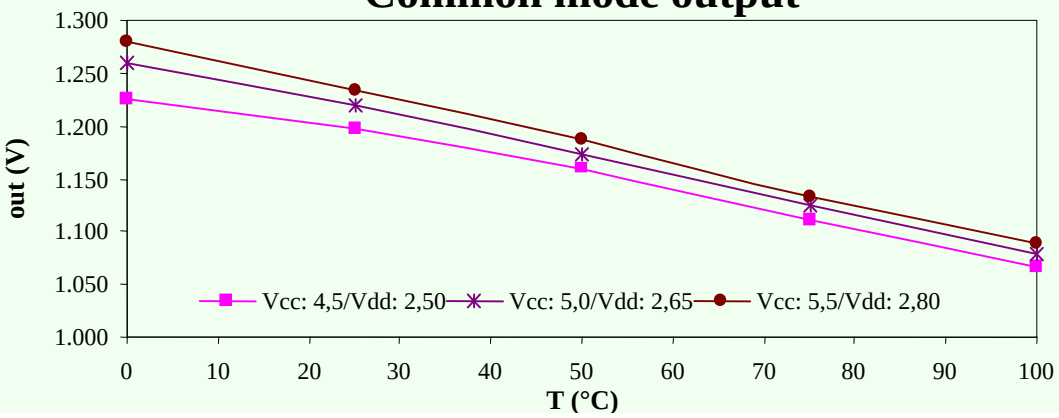
Pdd/channel



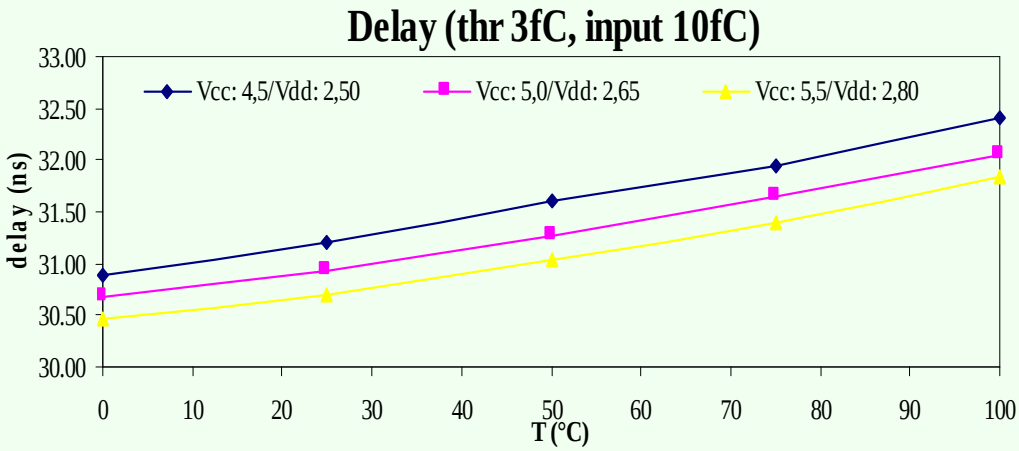
Differential output

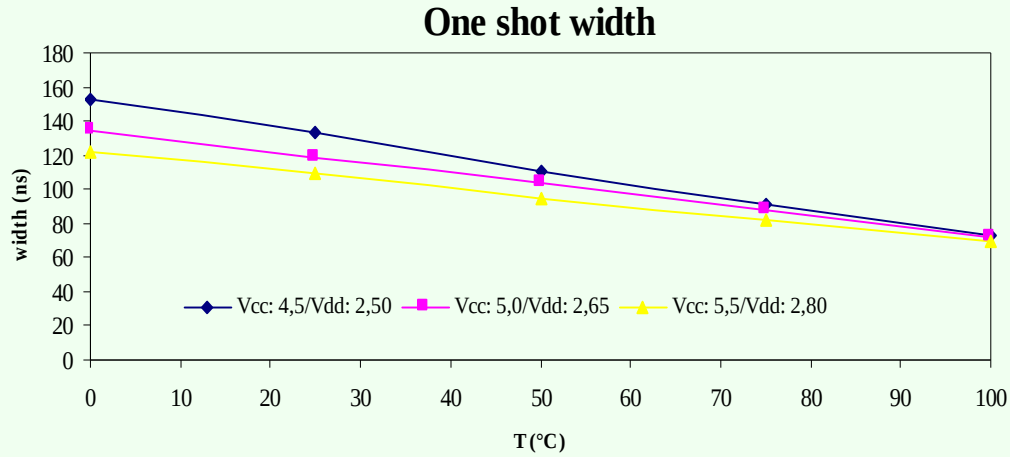


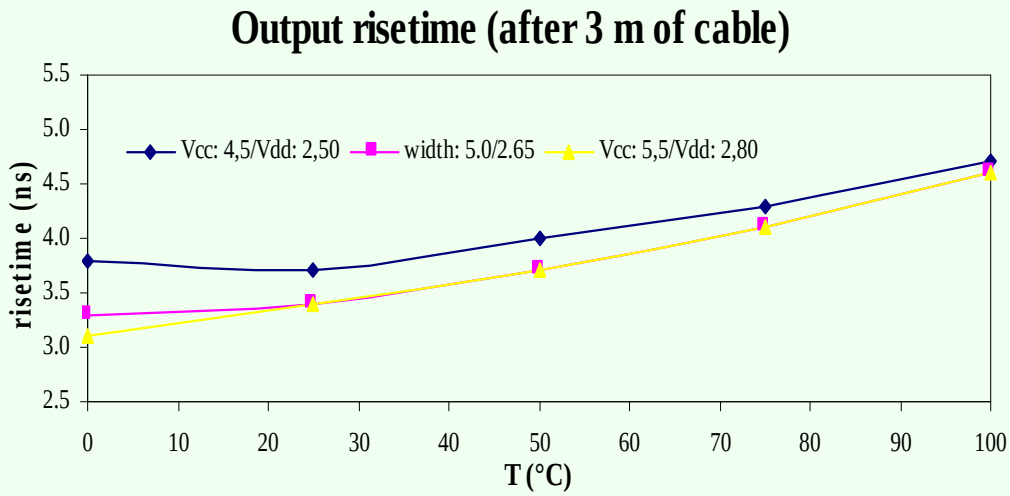
Common mode output

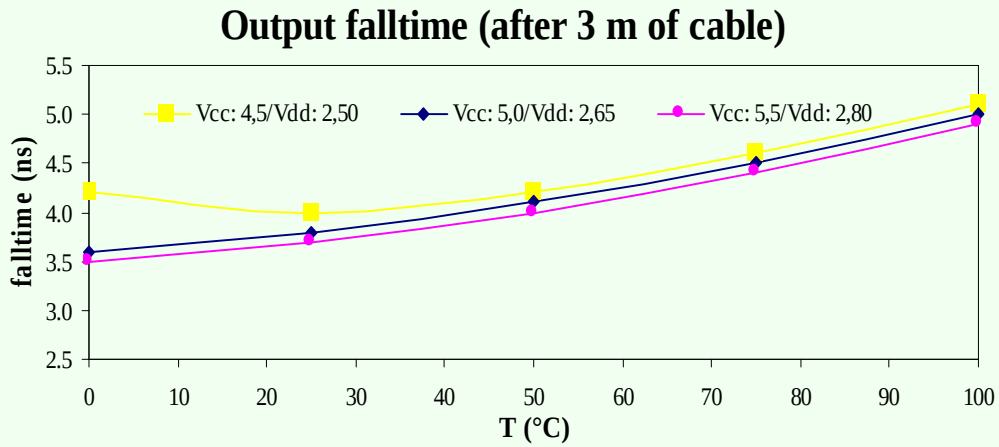


TEMP. & SUPPLY DEPENDENCE
Signal timing







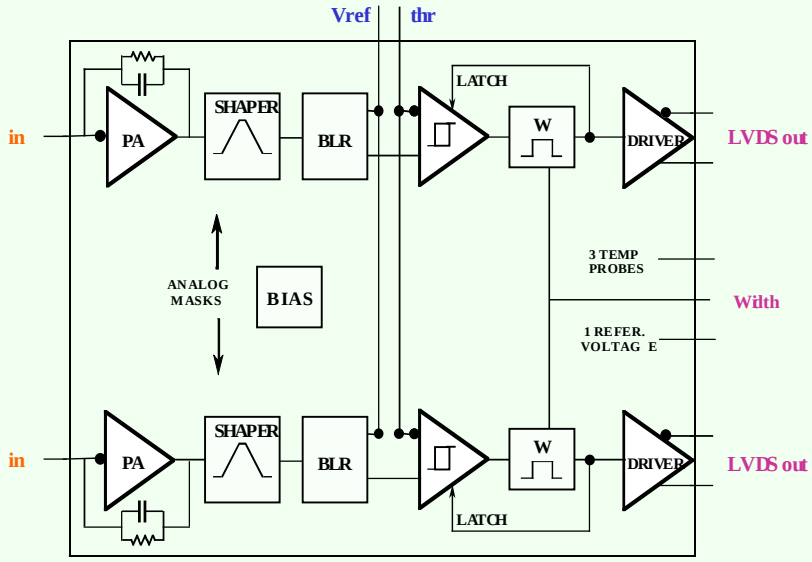


FRONTEND ROADMAP
What's done

NEXT STEPS TOWARDS FINAL CHIP

MADAUX CHIP :

The purpose is test of auxiliary functions:
_analog &digital masks
_temperature probes & voltage reference



CHARACTERISTICS

Two channel version of chip presently under test except for :

New insulation among different sections to improve crosstalk

Addition of 3 temperature sensors & 1 voltage reference

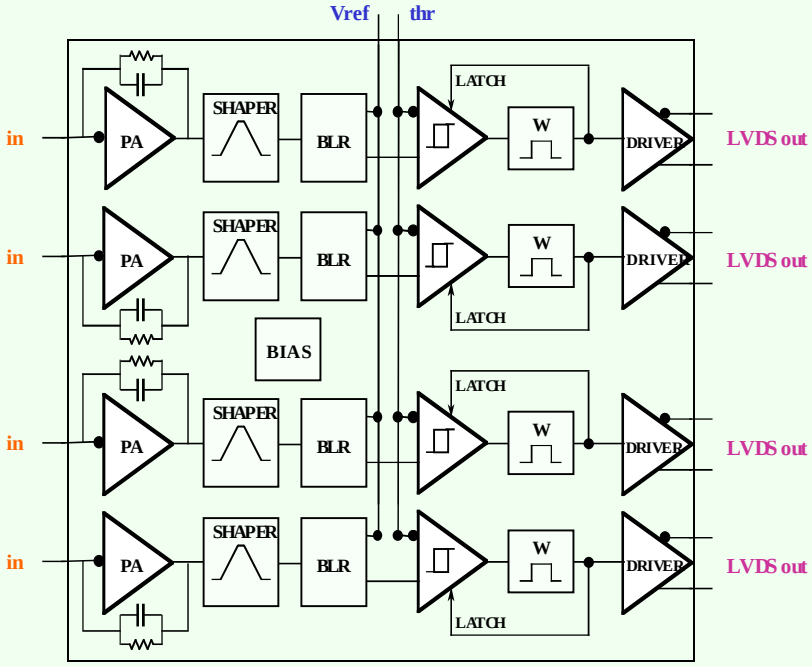
Addition of analog & digital mask

DELIVERY FORESEEN FOR MID MAY (should be today)

(10 PIECES UNTESTED)

MADIV CHIP :

The purpose is to equip a significant part of a prototype chamber



CHARACTERISTICS

Same as chip presently under test except for :

Slightly changed integration time

Addition of 1 temperature sensor

Improvements for threshold accuracy

Improvement for crosstalk

DELIVERY FORESEEN FOR MID JULY
(~ 100 PIECES UNTESTED)

FRONTEND ROADMAP
Conclusion

- After extensive tests of last two prototypes it will be possible to optimize this frontend to better suit the characteristics of the detector.

- Further work in the meanwhile will be carried on the following items:
  - Radiation tolerance
  - Protection to ESD
  - MTBF definition
  - Definition of test at wafer level.

- We plan to have another prototype run by the end of year in order to test the finalized design before mass production. This refined design should include all modifications (time constants, masks etc.) and also be packaged in QFP 44 (10 x 10 mm^2 final case).

- Tests are foreseen to be completed in April 99 and hopefully after that phase it will be possible to place the order for 200 K channels (70 K chips including spares).