A PROTOTYPE FRONTEND ASIC FOR THE DRIFT TUBES OF CMS MUON DETECTOR

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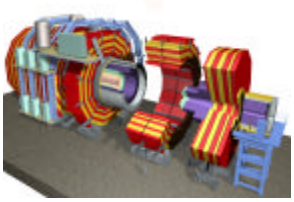
Compact Muon Solenoid

CMS is a general purpose proton-proton detector designed to run at the highest luminosity at the LHC (Large Hadron Collider).



The main design goals of CMS are:

i) a highly performant **muon system**
ii) the best possible **electromagnetic calorimeter** consistent with (i)
iii) a high quality **central tracking** to achieve i) and ii)
iv) hermetic **hadron calorimeter**

Detector Parameters - Frontend Design -

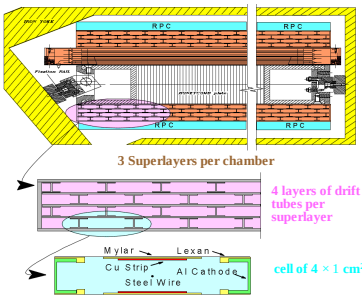
- Gas mixture $ArCO_2$ 85:15 @ atmospheric pressure
- Low gain (50 K÷100 K) for long lifetime
- Drift rate 55 mm/ns; max drift time 400 ns
- Maximum tube length 3 m; stainless steel wires f = 50 mm

Main goals are efficiency & time resolution

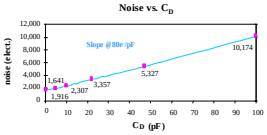
The frontend task is to amplify signals, discriminate them against an external threshold and transmit the results to data acquisition. This must be accomplished in the smallest space and consuming very little power.

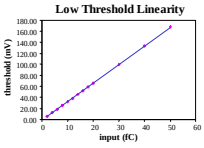
- Low noise, high gain analog chain.
- Fast rise time to minimise time walk due to different amplitude signals from drift tubes.
- Maximum uniformity among chips without equalisation at wafer or board level. Hence low offsets and little tolerance for gain.
- Built in hysteresis to improve speed and stability.
- Programmable output width independent from signal amplitude to override cable bandwidth.
- Fast, low level (LVDS compatible) cable driver to minimise power and interference.
- Other features for control & monitor purposes like the possibility of masking noisy channels and inclusion of a temperature sensor.

Barrel Muon Chamber

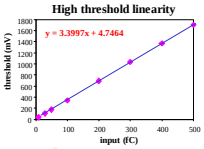


Noise and slope about 30% bigger than simulated: probable reason the input pad protection resistor.

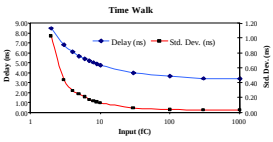


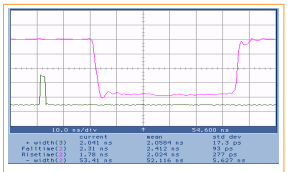


Low and high input signal threshold linearity. **Integral nonlinearity is less than 1%** (loss of gain < 6% below 10 fC, most probably caused by the finite gain of the discriminator).



Time walk about 3.5 ns @ threshold 1.5 fC (input charge range: 3 fC ÷ 1 pC).

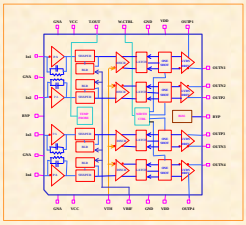




Minimum width of discriminator input signal: **2 ns pulses with 5 mV overdrive are captured with 99.9% efficiency**.
Actual behaviour is better as for this test we use the output of the shaper (with 1 mV r.m.s. noise) as reference for comparator.
Delay due to pulser trigger.

CROSSTALK

- **Maximum crosstalk found is 0.2% of the sum of the pulses applied to adjacent channels.**
  Crosstalk reduces to half cutting PCB trace to input of channel under test.
- **Interference from output driver to analog section turned out to be at noise level even when an unterminated cable (worst condition) is connected.**
- **Crosstalk on readout board is 0.3% in average and includes contribution of test pulse distribution.**



FRONTEND ASIC PROTOTYPE

Block diagram

Characteristics

- 0.8 mm BiCMOS technology by AMS
- 4 channels in 2.5 x 2.3 mm^2 die area housed in 28 pin CLCC J-type case
- 2 MPW production runs for 110 untested samples; 96 fully working
- Preamplifier GBW > 1GHz (simulation); P @ 2.5 mW
- Simple shaper, with short integration time, inside feedback loop of a low offset OTA
- Baseline and threshold levels common to all channels
- One shot activated latch
- Voltage output cable driver with LVDS compatible levels; termination resistors inside pads
- temperature sensor output 7.5 mV/ °K

Perfomances

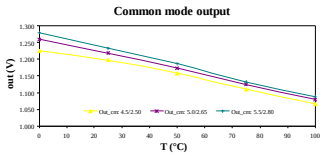
- 25 mW/ channel @ +5 V & +2.5 V (average of 56 chips) minimal variation with signal rate and temperature
- Zin @ 200 W (5÷200 MHz)
- noise @ 1600 e^- @ C_{in} = 0; slope @80 e^-/pF
- sensitivity @ 3.35 mV/fC ; capacitor tolerance (max 10%) affects uniformity for different batches
- baseline restorer + discriminator offset < 0.13 fC r.m.s.
- max input signal before saturation @800 fC
- threshold range 0 ÷ 500 fC with < 1% nonlinearity
- max input rate without loss of accuracy > 2 MHz @ 1pC
- crosstalk < 0.2%
- propagation delay 3.5 ns ; time walk 3.5 ns (3 fC ÷ 1 pC)
- output t_r & t_f < 2.5 ns
- temperature sensor error 3 °K @ 25 °C

Chip microphotography

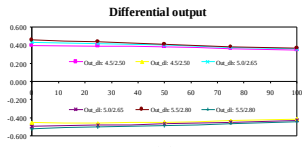
STATUS - CONCLUSIONS

- **Very good performances at low power. Also yield seems good: about 85% (on MPW run).**
- **Two runs used to equip a superlayer of drift tubes for test with muon beam. Analysis is in progress and preliminary results confirm bench tests.**
- **Improvements for next prototype :**
  - Noise dependence on C_D is somewhat worse than simulated: need more current at input stage (1.5 mW) and to remove the input pad protection resistor.
  - Noisy channels masking feature.
- **Further work need to be carried out on following items:**
  - Radiation tolerance to neutrons (already successfully tested).
  - Protection to ESD.
  - MTBF.
  - Definition of test at wafer level.

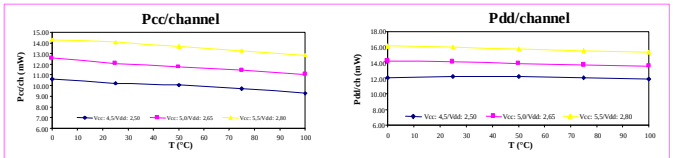
The final chip would be packaged in QFP 44 case (prototypes were packaged in CLCC 28).



Plot of the common mode differential output (120 Ω load) versus temperature for three power supply choices.

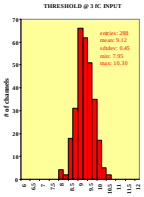


Plot of the differential output levels (120 Ω load) versus temperature for three power supply choices.

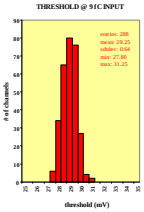


Total power dissipation: **25 mW/channel**
about 5% increase @ 1 MHz input signal rate

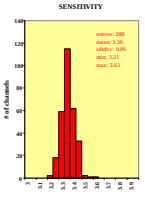
READOUT BOARDS OF A CHAMBER SUPERLAYER



Threshold uniformity distribution @ 3fC input charge.



Threshold uniformity distribution @ 9fC input charge.



Sensitivity distribution @ 6fC input charge.

TEST DATA FOR 18 BOARD

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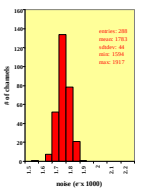
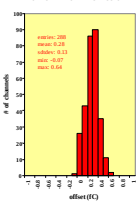
CHARACTERISTICS

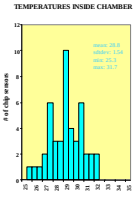
- 16 channels
- 155 x 45 mm^2; 4 layers
- I^2C interface for temperature readout & mask programming
- Double distribution of test pulse
- Additional protection diodes on inputs
- Total thickness (detector dead space) 20 mm (including input HV capacitor board)
- 1 superlayer of a typical chamber (56 chips) equipped Aug 98



Noise distribution @ ~4 pF input capacity



Total offset distribution: baseline restorer + comparator



Temperature distribution for boards inside chamber

Padova - October1998