A PROTOTYPE ASIC FRONTEND FOR THE MUON CHAMBERS OF CMS BARREL

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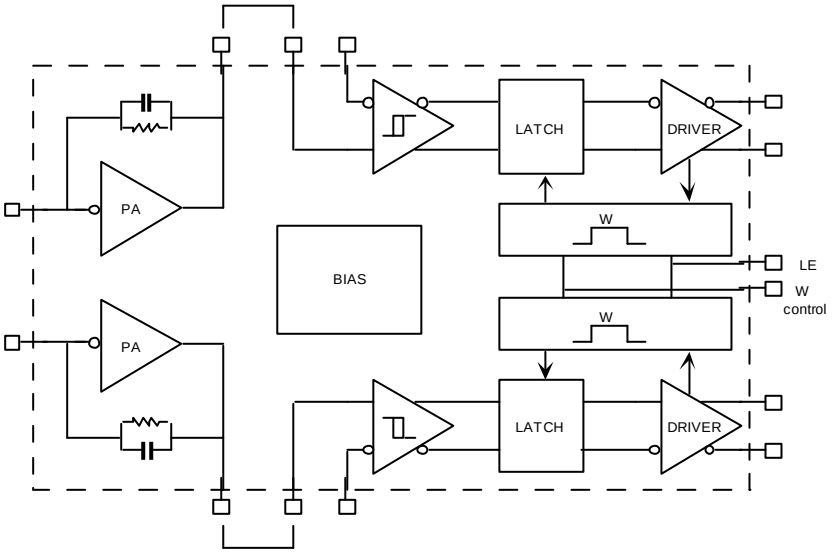
INTRODUCTION

A prototype custom chip has been produced (MAD chip) using AMS 1.2 µ BiCMOS technology; this integrated circuit contains 2 independent channels made of a charge preamplifier followed by a fast discriminator and a pulse stretcher, the output being able to drive long twisted pair cables. The main goal was to test the technology with special respect to speed, precision and power consumption in the perspective of integrating a large number of front end channels for the CMS barrel muon detector; very good performances have been obtained and the possibility of downscaling the design to 0.8 µ leaves room for improvements of all characteristics. Uniformity and tolerance to process variations have been checked by comparing chips from two different batches with resistor values in a 2:1 ratio (larger than maximum process spread).

DESCRIPTION

The chip is housed in a 28 pin CLCC (J type) package and divided in two symmetrical sections whose block diagram is the following:



Block diagram of MAD chip

The preamplifier is of the charge input type with a designed decay time constant of 50 ns and sensitivity of 2mV/fC (delta type input); simulations give a noise of about 1000 electrons r.m.s. @ 0 Cd with a slope of 50 electrons/pF (BW=500 MHz). It employs a mixed folded-unfolded cascode circuit with GBW=1 GHz (simulation) followed by an emitter follower that drives the output pad for a total of 4 mW power drain at 5V.
Maximum signal before saturation is 1 pC and input impedance is 180 ? in the range 2-200 MHz.

The discriminator is a rather classic one with latch; common mode input ranges between 1 and 4 Volt and hysteresis is designed to 2 mV in order to prevent noise retriggering. The output is level translated to feed the cable driver which is a low power differential one: it works from a 2.5 V supply and drives a 50+50 ? ground referred load to a level of 300+300 mV while consuming less than 20 mW. One tap in the driver triggers the one shot that, when active, enables the latch in order to catch the narrow pulses coming from the discriminator when the input is just over the threshold and stretch the output in such a way to overcome the bandwidth limitation of long cables. This "capture" function is externally enabled by a level applied to one pin and the duration of the one shot pulse is as well programmable in the range 20-150 ns by means of an external analog level.

In order to easily test the different parts of each chain the preamplifier is completely separated from the digital part (comparator, one shot and cable driver) and has an output pin which can be externally connected to the discriminator input. Also power supplies are separated even if during tests the analog and the digital parts shared the same supply without interfering each other.

TESTS

As already mentioned, two MPW production runs have been made for this chip, the first one being affected by a boolean error during mask processing: this error brought to resistor values lower by a factor of 2 than designed. The number of samples was limited to 10 while in the second run, having nominal values, 80 prototypes were processed.

The main difference between the two versions was a higher power consumption, about 40 mW for the chips of the first run compared to 30 mW measured on the others; other performances, like speed or noise, changed only slightly.

Untested parts were delivered for both runs and we found that a total of 76 integrated circuits were fully functional .

The preamplifiers were first tested in both versions for noise, rise time and input impedance characteristics.

Noise turned out to be a little lower than simulated, this can be explained by the small capacitance of the scope and the short cable used to connect it to the preamplifier output that reduces the measurement bandwidth (nominally 500 KHz - 500 Mhz).

Results are the following (typical):

nominal values	ENC = (1000 + 40/pF) electrons
reduced values	ENC = (1150 + 34/pF) electrons

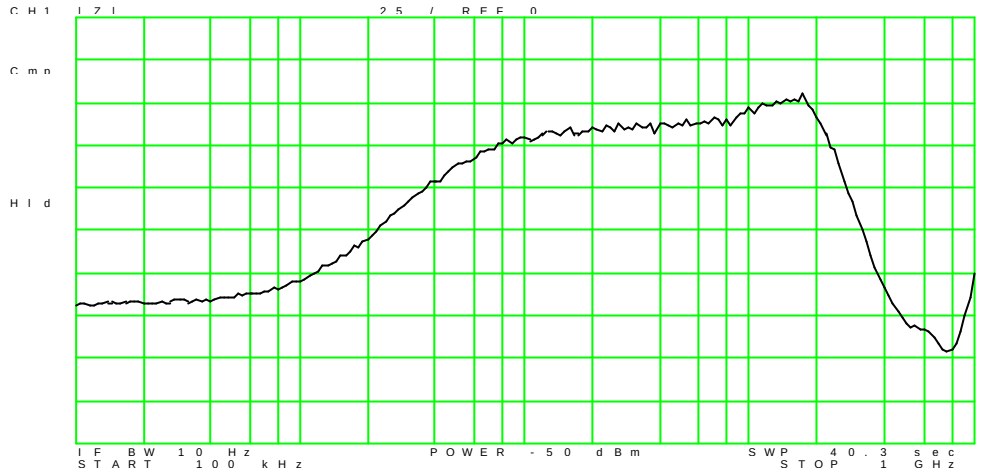
Rise time test was affected as well by the capacitance problem and the results were somewhat worse than expected:

nominal values	tr = (3.5 + 0.3/pF) ns
reduced values	tr = (3.0 + 0.17/pF) ns

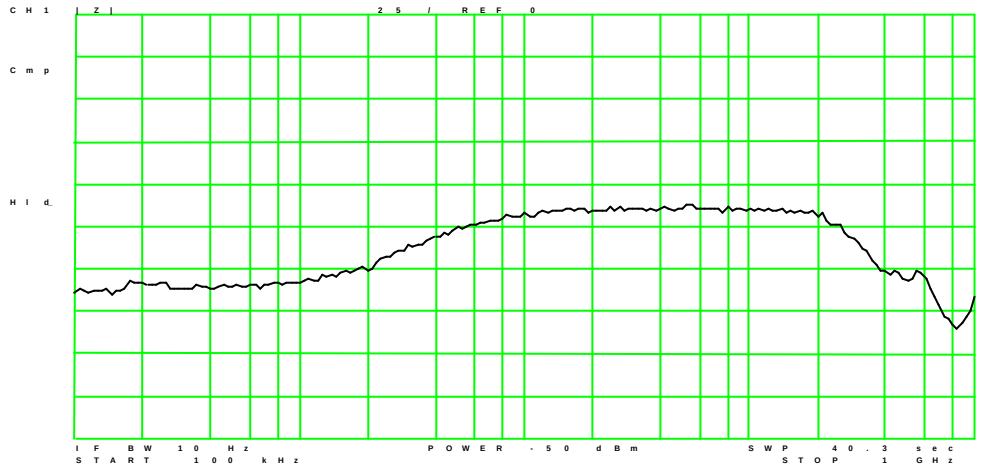
Input impedance has been measured using an HP 4393 network/spectrum analyzer in the frequency range 100 KHz - 1 Ghz.The resulting plots for the two versions are shown in the next page

Agreement with simulation is very good except for f > 200 MHz where small input parasytic capacitances produce big effects. The low value at low f is not critical for drift tubes where wires and preamplifiers are connected through capacitors of about 1nF.

MAD 30 mW



MAD 40 mW



Horizontal scale starts at 100 KHz and ends at 1 GHz
Vertical scale is 25 ? /div starting at 0 ?

Sensitivity was measured to be 2.1 mV/fC in average at zero detector capacitance and the slew rate about 400 V/μs.

The only problem found in the preamplifier is the rather high (1%) crosstalk between the two channels that is likely caused by a missing internal ground connection and by the large test pads that were inserted in the chip to check the operating point of the preamplifier.

The digital section was extensively tested for static and dynamic characteristics according to the table in the following page which reports the results of a reduced value resistors chip.

DISCRIMINATOR SECTION

Temp	Vdd	Hysteresis(mV)	Offset(uV)	Vcm min	Vcm max
Ta	5	2	-324	0.84	4
Ta	5.5	2.2	-355	0.83	4.5
Ta	4.5	1.4	-340	0.84	3.5
0°	5	2.5	-292		
0°	5.5	2.9	-300		
0°	4.5	2	-300		
70°	5	0.92	-350		
70°	5.5	1.17	-357		
70°	4.5	0.62	-351		

Vin step	Tpd(ns)
10mV	2.5
100mV	2.3
1V	2.5

Temp	Vdd	Tpd(ns) Fast input	Tr(ns) Fast input	Tf(ns) Fast input	Tr(ns) Slow input
Ta	5	3	1.7	1.6	2.3
Ta	5.5	3	1.9	1.8	2.3
Ta	4.5	3	1.9	1.8	2.6
0°	5	2.3	1.6	1.5	1.95
0°	5.5	2.3	1.6	1.6	1.9
0°	4.5	2.5	1.6	1.5	2
70°	5	2.8	2	1.8	6.1
70°	5.5	2.5	2	1.8	5.3
70°	4.5	2.9	2.1	1.9	8

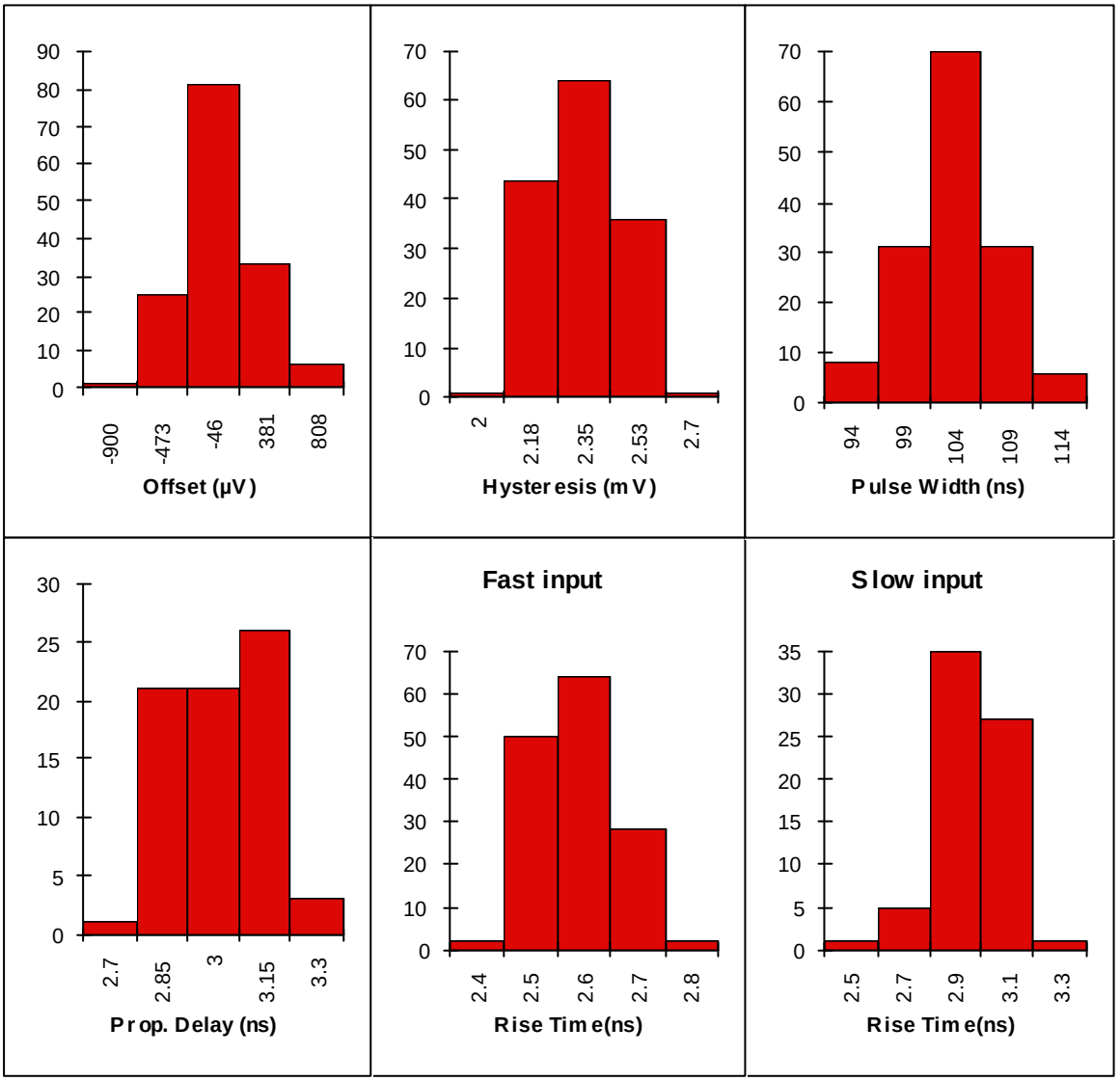
Temp	Vout H(mV)	Vout L(mV)	Fmax(MHz)
Ta	300	8	181
0°	296	4	227
70°	270	10	172

ONE SHOT SECTION

Temp	Vdd	Vcontrol	Width(ns)	Dead time(ns)
Ta	5	3.299	99	14
Ta	5.3	"	106	15
Ta	4.5	"	90	13
0°	5	"	167	21
0°	5.3	"	179	28
0°	4.5	"	141	18
70°	5	"	55	12
70°	5.3	"		
70°	4.5	"	51	14

In this table slow input refers to an input signal having a slew rate of 1mV/µs that was used to test the efficacy of the hysteresis either in speeding up the circuit either in eliminating input-output interference that could result in oscillations when the signal is small and slow. Dead time is the time required by the one shot to reset completely after one pulse has finished (after that time an input pulse produces again a full width output). As one can see performances are very similar to commercial products that require much more power; also, temperature & supply variations do not affect most of them in a significant way.

Tests performed on the digital section of the nominal value resistor chips show very little spread in the most important parameters as demonstrated by the following plots:



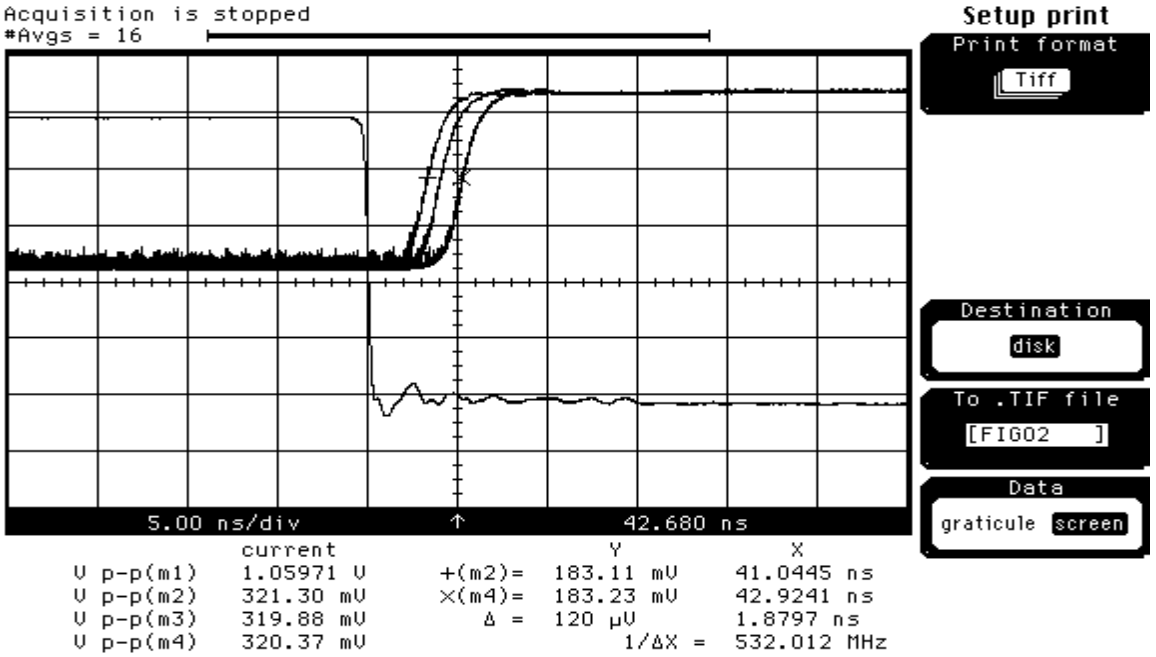
vertical axes represent the number of channels

A very important characteristic of a readout chain for our application is the uniformity of the threshold among all channels: a little spread allows to operate at low threshold so improving the time resolution and keeping low the gain of the drift tubes. From these plots one can see that the spread, caused in the discriminator by the offset and hysteresis distributions, is less than 1mV r.m.s. or 0.5 fC when the preamplifier is connected without further amplification to the discriminator .

The propagation delay distribution also shows little spread, about 0.1 ns r.m.s.

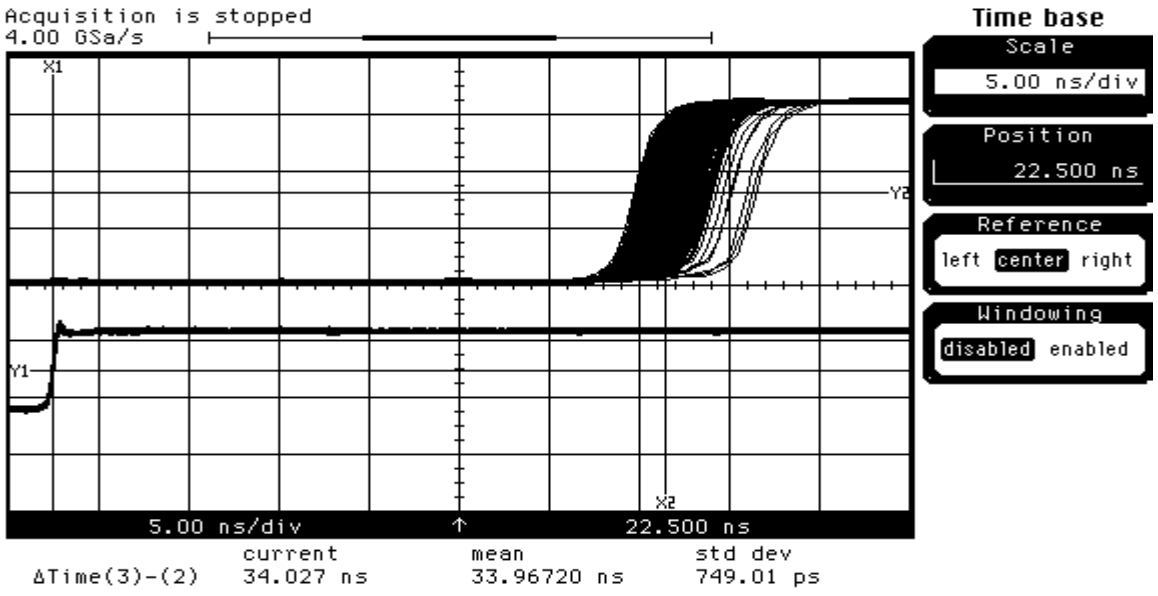
Next step of our tests was to connect capacitively the preamplifier to the discriminator and measure the overall performance: next picture shows the propagation delay of the chain under different input charge values keeping the threshold at a constant value. The effective input charge is obtained by subtracting half of the comparator hysteresis (.5 fC) from the input delta current signal

MAD 30 mW preamplifier + discriminator propagation delay @ thr = 1.5 fC
input before attenuation & output shown
effective inputs 2.5 fC, 10 fC & 1 pC
time walk < 2 ns

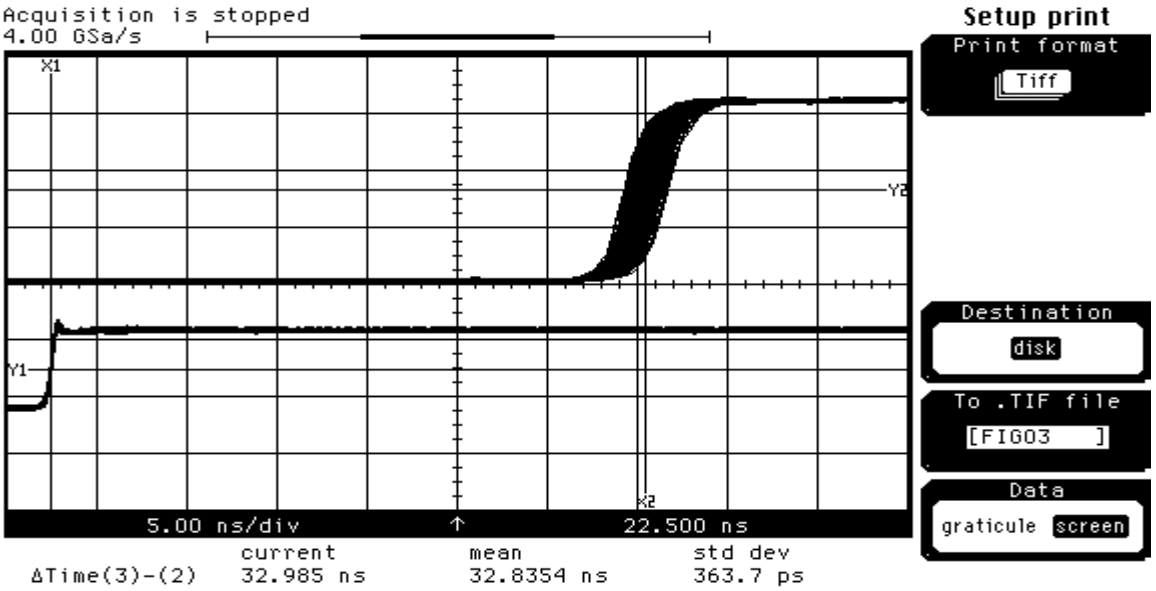


The following pictures show the intrinsic time resolution limited by the preamplifier and discriminator noise evaluated for 1 chip; also in this case the effective input charge is considered while threshold has been set at the lowest attainable value (0.5 fC) for all measures.

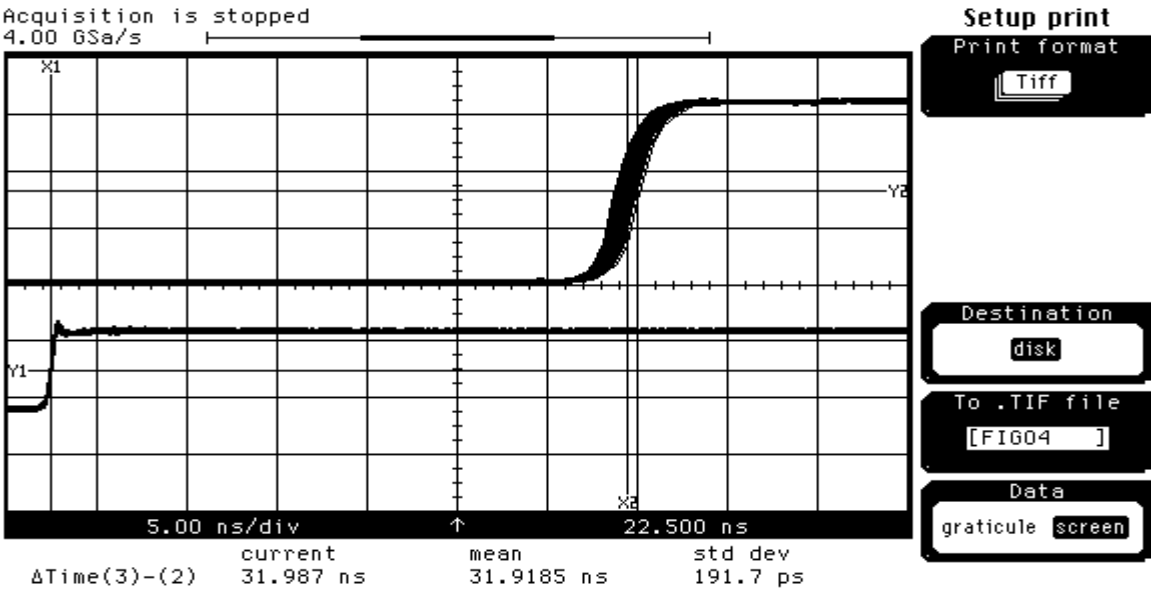
MAD 30 mW prop. delay @ 1fC : mean = 34 ns; r.m.s.= 0.75 ns
(trigger source + cables account for ~ 26 ns)



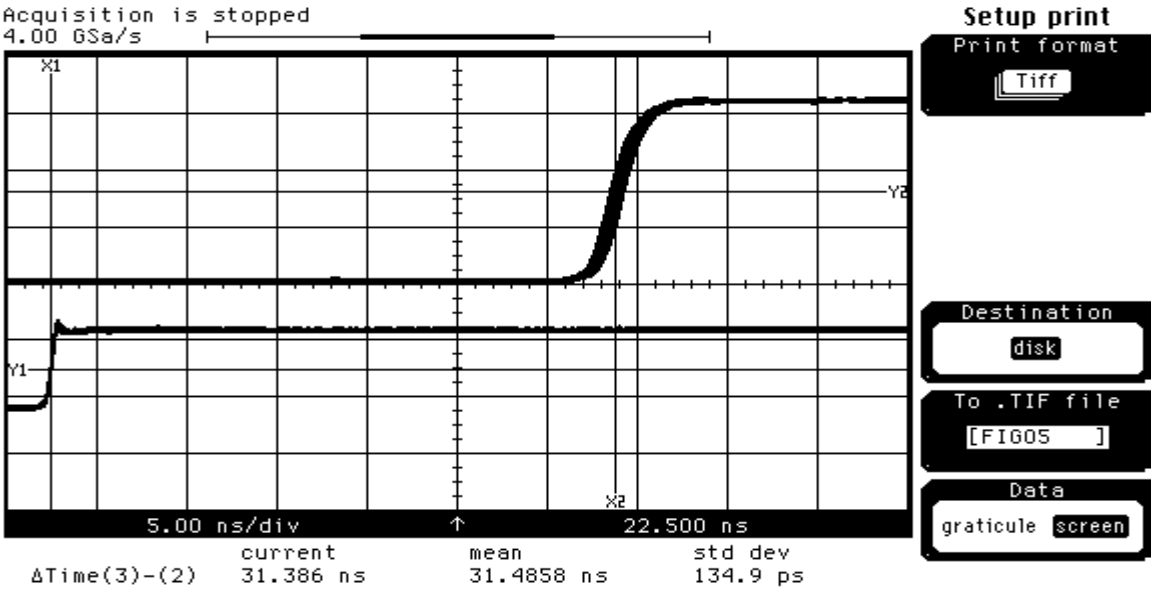
MAD 30 mW prop. delay @ 1.5 fC : mean = 32.8 ns; r.m.s.= 0.36 ns
(trigger source + cables account for ~ 26 ns)



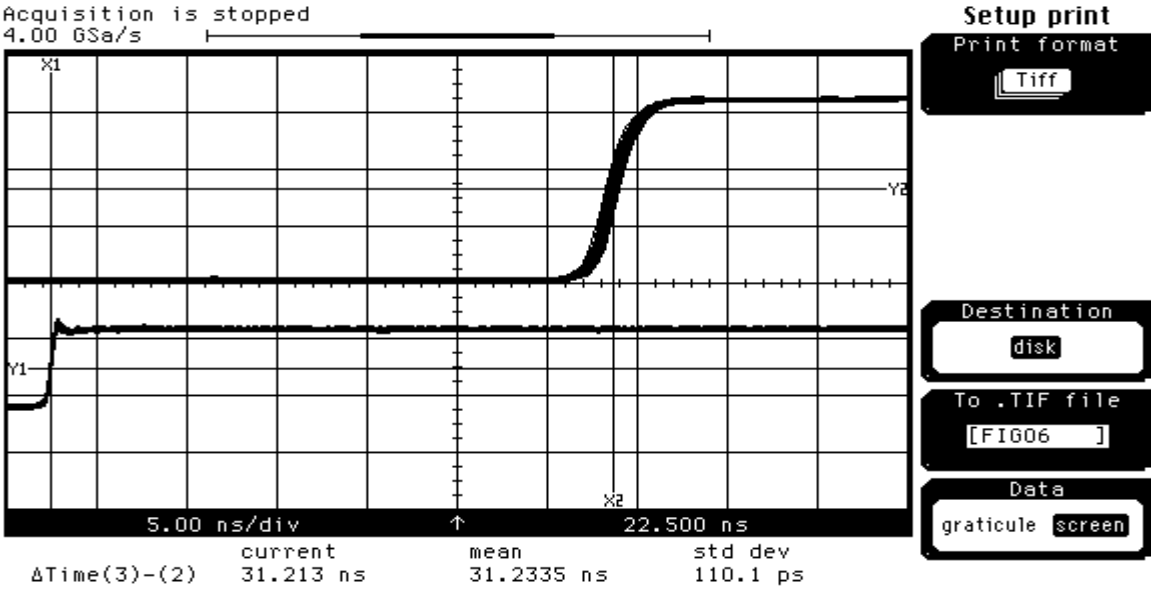
MAD 30 mW prop. delay @ 2.5 fC : mean = 31.9 ns; r.m.s.= 0.19 ns
(trigger source + cables account for ~ 26 ns)



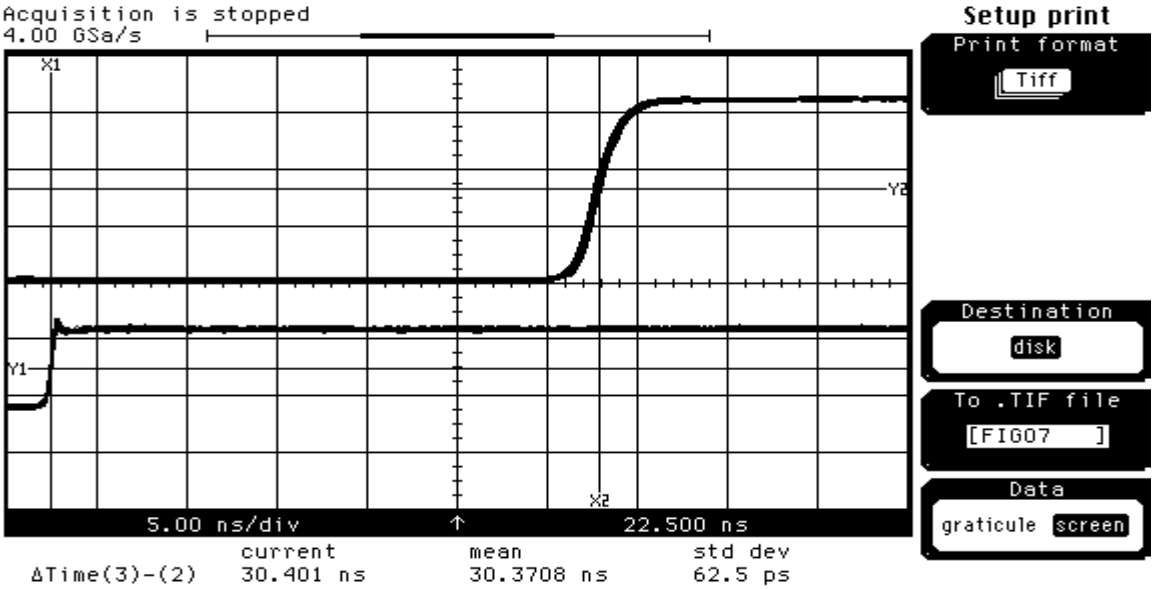
MAD 30 mW prop. delay @ 3.5 fC : mean = 31.5 ns; r.m.s.= 0.14 ns
(trigger source + cables account for ~ 26 ns)



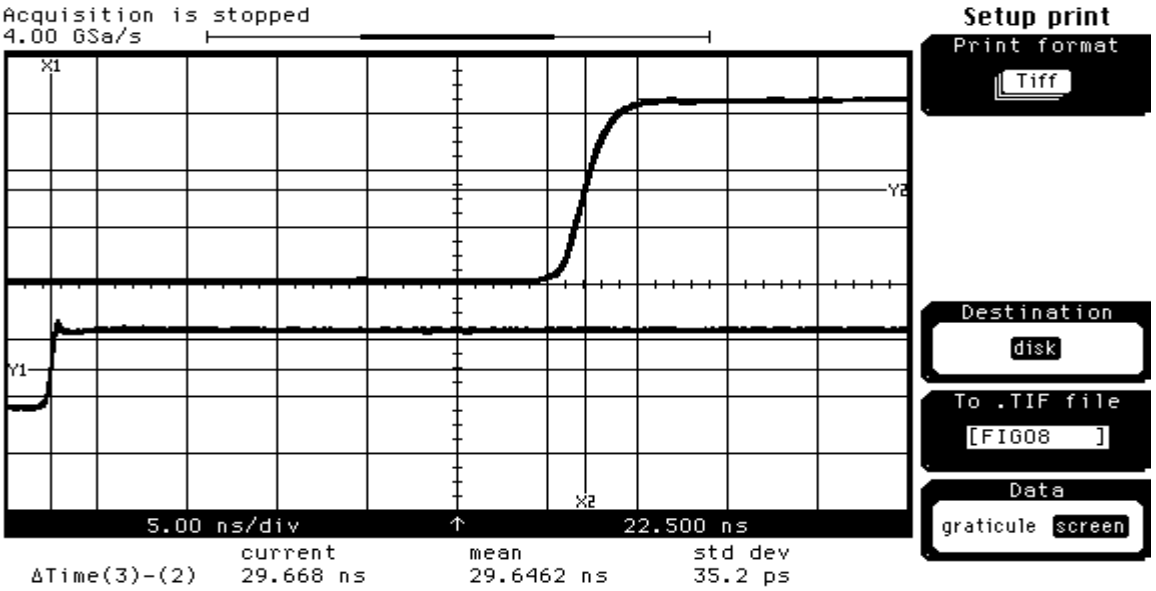
MAD 30 mW prop. delay @ 4.5 fC : mean = 31.2 ns; r.m.s.= 0.11 ns
(trigger source + cables account for ~ 26 ns)



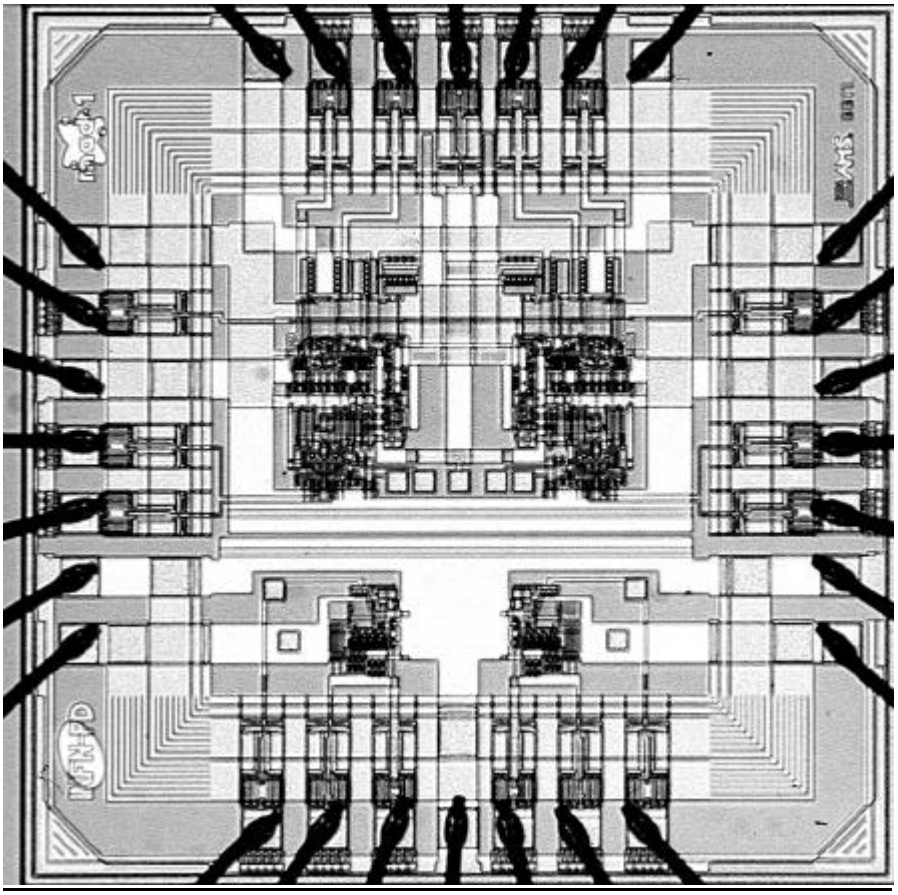
MAD 30 mW prop. delay @ 10 fC : mean = 30.4 ns; r.m.s.= 63 ps
(trigger source + cables account for ~ 26 ns)



MAD 30 mW prop. delay @ .1 pC : mean = 29.65 ns; r.m.s.= 35 ps
(trigger source + cables account for ~ 26 ns)



From these pictures one can see that most of the time walk occur for input signals ranging from 1 to 10 fC where the delay between the trigger of the pulse generator and the output from the MAD changes of 3.6 ns.



Micrograph of MAD chip

CONCLUSIONS

This prototype, although not complete, has demonstrated the feasibility of integrating in a single chip more channels of fast electronics for the readout of drift tubes while keeping very low power dissipation.

Chip size is very little, the core area for 2 channels is 1.5 sq.mm, and a possible scaling to 0.8 µ technology would reduce also the power requirements.

The preamplifier has shown very good performances that could be improved by adding some simple signal processing and a gas tail cancellation network, while the crosstalk can be cured with one additional ground connection.

The digital section is fast, with a bandwidth larger than 150 Mhz, doesn' t show autoscillation problems even with slow inputs and is able to capture very narrow pulses.

The sensitivity to process tolerances is rather little and allows to operate at low thresholds.

A possible improvement could be the implementation of an LVDS output stage with the advantage of adopting standard cells in the receivers at the other side of the cables. Another feature that could be very useful is the possibility of masking noisy channels by remotely programming one register: this can be easily implemented using standard cells already available in AMS BiCMOS technology.