A PROTOTYPE FRONTEND ASIC FOR THE READOUT OF THE DRIFT TUBES OF CMS BARREL MUON CHAMBERS

F.Gonella and M.Pegoraro
INFN Sezione di Padova, Via Marzolo 8, 35131 Padova ITALIA
e_mail: franco.gonella@pd.infn.it; matteo.pegoraro@pd.infn.it

Abstract

A full custom ASIC prototype, integrating the basic frontend electronics for the muon drift tubes of CMS barrel, has been produced and tested.

The task of this IC is to amplify signals picked up by chamber wires, compare them against an external threshold and transmit the results to the acquisition electronics. The working conditions of the detector set requirements for high sensitivity and speed combined with low noise and little power consumption.

We used 0.8 µm BiCMOS technology by Austria Mikro Systeme for this application as it provides most of the basic components and simulation parameters needed for analog designs; also the possibility of mixing high speed NPN bipolar transistors with CMOS devices and standard cells allows one to increase functionality.

As the basic requirement for the frontend is the ability to work at very low threshold to improve efficiency and time resolution, a good uniformity for sensitivity and threshold setting is needed; cost and space reasons force us to attain this goal without any equalization at wafer or board level so special care was taken at design phase to minimize offsets and mismatches.

The prototypes were produced in 100 samples partly used to read out 224 drift tubes (one third of a typical CMS chamber) that were tested with a muon beam in mid August 98. Data are now being analyzed and preliminary results confirm that most of the goals have been reached.

1. CIRCUIT DESCRIPTION

1.1 General

The block diagram and pinout of the ASIC are shown in Figure 1.

One integrated circuit contains 4 complete analog chains, each made of a charge preamplifier and a simple shaper with baseline restorer, whose output is compared with an external threshold by a latched discriminator; the output pulses are then stretched by a programmable one shot and sent to an output stage able to drive long twisted pair cables with LVDS compatible levels.

Also included are a bias voltage source common to all channels and a temperature sensor for slow control purposes.

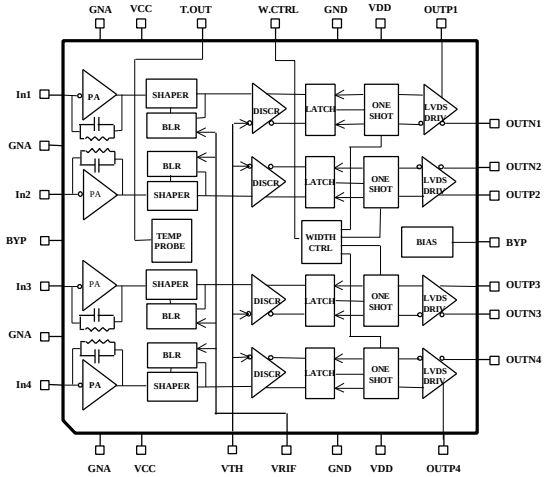

Figure 1: block diagram of prototype ASIC

1.2 Analog section

The preamplifier uses a single gain stage with a simulated GBW product in excess of 1 GHz and a feedback time constant of 32 ns. Input is protected against ESD by an integrated resistor and diodes connected to the ground and to a voltage of about 2 Vbe generated internally. Power dissipation for the whole stage is 2.5 mW.

The shaper is a low gain integrator with a small time constant: the noninverting input is connected to the preamplifier while the inverting one makes it possible to put this stage inside the feedback loop of a low offset OTA; this combination implements a time invariant baseline restorer acting as a high pass filter for the signal path. Tests performed on this circuit show that the quiescent level of shaper output can be set anywhere between 1.0 and 3.5 V even in the presence of worst case parameters for fabrication process and operating conditions of the IC. A pin common to the four OTAs is used to control this level from outside.

The output of the shaper is directly connected to the noninverting input of a fully differential discriminator with 2 gain stages. The other input of the comparator is connected to an external threshold pin common to all

channels. The input section uses no special technique, except a careful layout, to obtain low offset with high speed; an hysteresis of about ±1 mV helps in avoiding autoscillation and in speeding up commutation with slow input signals. Common mode input voltage ranges from 1.2 to 3.8 V. Finally, a buffer prevents switching noise from the following sections to propagate backwards to sensitive paths.

All previously described blocks share a single +5 V supply for about 12 mW power drain.

1.3 Digital section

The buffered output of the discriminator is capacitively coupled to a one shot that is very similar to a classical astable multivibrator; its differential output, when active, stores the status of comparator in the latch so producing a non retriggerable pulse whose width is controlled by a current charging a capacitor. Critical parameters of this section are propagation delay, which sets the ability to catch narrow pulses produced by signals just over threshold, and the time it takes to fully recover after the falling edge of a pulse.

The same lines that activate the latch are used to feed the output driver, again a differential one capable of driving a 100 Ω load at voltage levels compatible with LVDS standard. Voltage driving has been chosen because NPN bipolar transistors are faster than PNP and PMOS devices and also because it is power convenient when the load is a cable terminated at both ends. Working conditions of the driver are a compromise between speed and power drain, rise and fall time are below 2.5 ns and, to reduce external components, terminating resistors are integrated in the pads. To reduce consumption, the supply voltage is the lowest possible, 2.5 V, for a power dissipation, including the one shot, of about 12 mW.

1.4 Temperature Sensor and biasing

Temperature sensor is based on voltage difference between base emitter junctions operated at different current densities. Voltage output is 7.5 mV/^{o}K and power drain about 1 mW from 5 V.

Bias circuit controls current generators of the whole chip and supplies voltage for one shot sections.

2. TESTS AND PERFORMANCES

2.1 Acceptance and Yield

This circuit was submitted to a MPW run in mid April 98 and 100 untested samples were delivered in mid July. A first screening test, based just on the measurement of pin voltages and supply currents and on detecting response to a charge pulse, was passed by 88 chips; a more refined procedure revealed that 1 further chip was out of specifications (one channel offset ≅ 2 fC).

Using 72 prototypes 18 readout boards were built to equip a portion of a full scale prototype chamber tested in the Gamma Irradiation Facility at CERN SPS; during the run another channel underwent failure so reducing the number of working ASICs to 86 out of 100.

2.2 Analog performances

Power dissipation was easily measured directly on the chamber portion with readout boards: 224 channels required 5.2 W total power almost equally split between +5 V & +2.5 V thus giving an average power drain of less than 25 mW/ch. Tests performed on a single chip showed that this figure changes at few percent level when pulsing the inputs at rates of 1 MHz and also that there is little dependence on temperature.

Since no test pads have been included in the chip, tests on analog section are based on the statistics of output response to charge pulses, so reproducing normal detector operation except for input stimuli that are now δ–like.

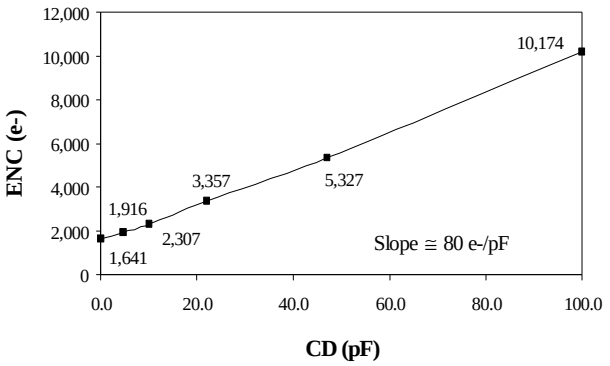

Figure 2: ENC vs C_D

Figure 2 shows typical noise performance as a function of detector capacitance: starting point is ENC ≅ 1600 e^- @ 0 pF and the slope is about 80 e^-/pF, rather high values not in complete agreement with simulations. This effect is mainly caused by the resistor (50÷100 Ω), integrated in input pads for protection, that affects both noise and sensitivity specially in the presence of large capacitance at preamplifier input. Input impedance is also increased by this component: its value is about 120 Ω from DC to 1 MHz and increases up to 200 Ω for frequencies ranging between 5 and 200 MHz; beyond this value it is dominated by parasitic capacitance at input.

Gain has been measured at zero detector capacitance and the typical performance is shown in Figure 3 for input charge pulses from 2 to 50 fC; the linearity is fairly good even if in the first part of the range (2÷10 fC) there is a slight decrease (≅ 6%) of sensitivity which is most probably caused by the finite gain of the discriminator. The mean value in the range is 3.4 mV/fC and is

constant up to 500 fC input with less than 1% integral nonlinearity. For higher values there is a loss of gain due to slew rate limitations while saturation occurs at about 800 fC.

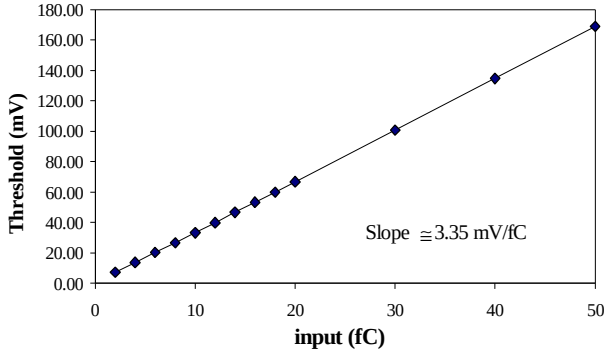

Figure 3: low threshold linearity

Gain and noise have been measured on 72 prototype chips equipping 18 readout boards: in this case some 4 pF of additional capacitance (protection diodes, input connector and test pulse capacitors) are connected to the input node and slightly increase noise. Figure 4 herebelow shows ENC evaluated on 288 channels.

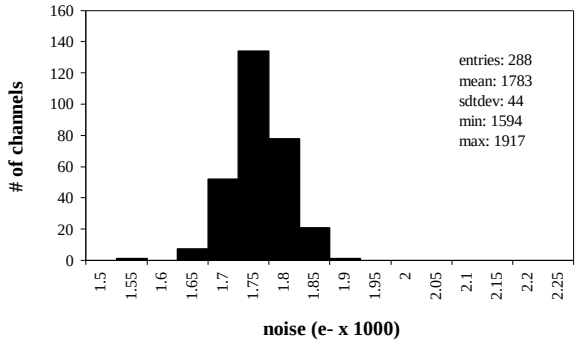

Figure 4: noise performance

In order to investigate the gain, two different values of charge, 3 and 9 fC, have been injected: the resulting threshold distributions have mean values of 9 and 29 mV, respectively, with r.m.s. of 0.45 and 0.64 mV. This small spread is due to gain variations among chips, caused by tolerance (max ±10% from process parameters) of feedback capacitor in charge preamplifier, and by discriminator and BLR offset. The former is unpredictable for chips produced in different sectors of a wafer or in different batches and expected to be dominant for high threshold values.

For low input charges the latter contribution can be the most important cause of threshold inaccuracy and in our case it can be calculated extrapolating, for each channel, the threshold characteristic to 0 mV: the 0 intersection, expressed in fC, shows a distribution, given in Figure 5, whose r.m.s. represents the effect of offsets on threshold inaccuracy. This interpolation, calculated again for 288 channels, is characterised by an r.m.s. of 0.13 fC corresponding to 0.44 mV.

This results ensure that, for example, for a threshold set to 3 fC, the error due to offsets is more or less equal to that caused by tolerance in gain.

Rate of input signals may also affect accuracy as the width of the shaper signal is given by preamplifier decay time and baseline restorer requires a certain time to recover from a large input pulse thus producing some shift of DC level. A test for this characteristic has been made by pulsing one channel via a capacitor with 3 fC charges and setting the threshold to detect 50% of charges rate. Then additional pulses of 800 fC have been injected, using a pin photodiode, in such a way that the capacitor injection occurred with 500 ns delay respect to light flash. No appreciable difference, as predicted by simulation, in the percentage of detection of capacitor pulses was measured with light flashing up to a frequency of about 2 Mhz. This represents a good safety margin taking into account that the maximum rate foreseen for a drift tube is around 10 KHz.

Crosstalk has also been measured on some samples on test boards and on a complete readout board. In the first case the maximum signal induced by neighbours on the channel under test was found to be 0.2% of the total input charge, and half of this figure is due to PCB traces. Signal feedthrough from output drivers is also very low, not distinguishable from noise, even in the worst condition, when an unterminated cable is connected to the chip. These results slightly change in the readout board where the average crosstalk is somewhat lower than 0.3% with a maximum of 0.5% for the channel physically located close to output flat cable.

From above measurements it turns out that a very good precision and accuracy in threshold has been achieved, not spoiled by working conditions even for very small input signals.

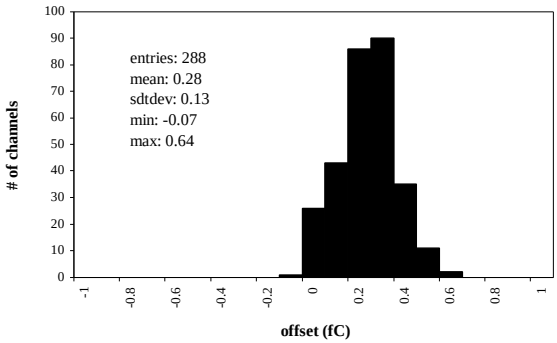

Figure 5: interpolation of threshold to 0 mV

2.3 Timing

Timing performances have been measured on a small test board carrying a single ASIC using an oscilloscope HP54720A and a pulse generator HP8131A. Time walk has been first evaluated: charge pulses of amplitude ranging between 2 fC and 1 pC have been injected with threshold set at about 1.5 fC: response times are shown in Figure 6.

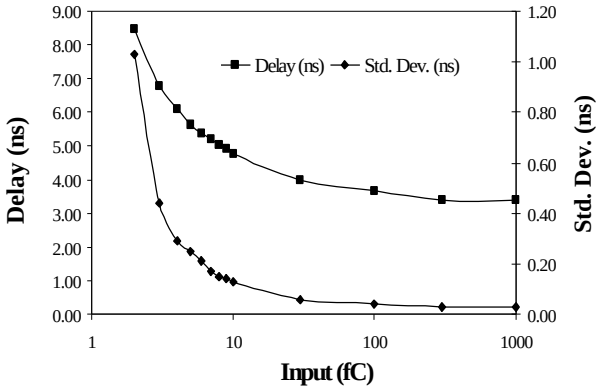

Figure 6: Time walk

Input to output propagation delay of the whole chip for the strongest signal is 3.4 ns and rises to 6.8 ns for an input charge of 3 fC; the actual time walk is obtained from this difference in delay by subtracting half of the pulse generator rise time, in this case 0.7 ns, and is about 3 ns. The r.m.s. of all measuring points, that for the same range increases from 30 ps to 0.4 ns due to input noise, is also plotted in Figure 6. The 2 fC point is strongly affected by noise and presumably also the delay value (8.5 ns) is worsened by this factor.

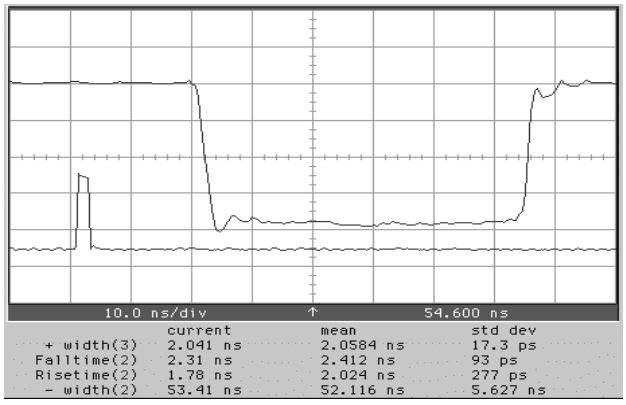

Figure 7: Narrow pulse capture

The oscilloscope photograph in Figure 7 summarises many critical performances of the digital section of the chip: for this test a negative pulse was applied to the threshold input of the discriminators while using the output of the shaper as reference level. The aim was to measure the minimum width and height for a pulse to be captured by the chain made by the comparator, latch and one shot, and to generate a stretched output from the cable driver. The result is that for an overdrive of 5 mV (including hysteresis) the pulse is detected with 99.9% efficiency when its width is greater than 2 ns. This is a rather conservative assessment as the reference voltage for the discriminator (the shaper output) has about 1 mV r.m.s. of noise superimposed. This performance gives also a rough estimate of the bandwidth used for noise tests based on the distribution of response to stimuli. Also shown in this photograph are the rise and fall times of the LVDS output: less than 2.5 ns with such a low amplitude input. The driver has been tested with cables up to 40 meter long connected to a standard LVDS receiver: the signal is recovered with a rise time of about 1 ns in all cases.

The one shot duration in this setup has been programmed to about 50 ns and, from other tests, is found to be dependent at the percent level on input signals ranging from 3 fC to 1 pC; width uniformity, measured on 56 chips, has an r.m.s. of about 5% while dead time is about 10 ns almost independent on programmed pulse duration.

All timing performances, except for the one shot width, exhibit little variations against temperature and the output levels comply with LVDS standard in the 0÷100 ^{o}C range and for supply voltage tolerances of ±10%.

2.2 Other Tests

Temperature sensors integrated in the ASICs were tested in the chamber used during August run; no cooling system was foreseen as the power consumption was little and the detector was in free air. Temperature readout was made with a multiplexer addressed via the I^2C interface of the frontend board. Figure 8 shows the distribution of readings for an ambient temperature of about 24 ^{o}C.

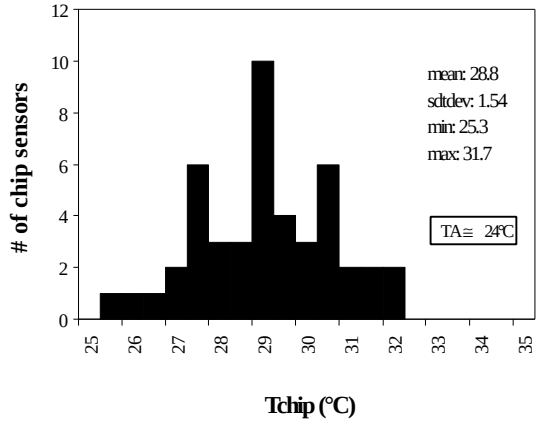

Figure 8: Temperatures inside superlayer

The rise in temperature respect to ambient is about 5 ^{o}C and measuring error is a maximum of ±3 ^{o}C; the conversion factor of 7.5 mV/^{o}K has been checked with a different setup in which a few ASICs have been put inside a climatic chamber and temperature output sampled in the range of 0÷100 ^{o}C in 25 ^{o}C steps.

3. CONCLUSIONS

Bench tests on the analog and timing sections of this prototype chip have revealed very good performances summarised in Table 1.

A statistically significant sample of devices was used to equip a portion of a full scale chamber for a run with muon beam; data analysis is in progress and preliminary results show good efficiency and time resolution as expected.

The production yield, evaluated on a MPW run, has been more than acceptable.

The final chip will include some features and improvements that will be first tested in a prototype whose submission is foreseen before end of this year; main changes will concern:

- input protection resistor will be moved outside chip in order to reduce noise in excess; for the same reason input stage current will be increased at the expense of 1.5 mW additional power drain;
- a mask circuit with minimal feedthrough on signal path will be implemented.

Further work will also be carried out on radiation tolerance and definition of test at wafer level before mass production.

Table 1: ASIC performances

power ≅ 25 mW/channel @ +5 V & +2.5 V	**threshold range** 0÷500 fC with < 1% nonlinearity
Zin ≅ 200 Ω (5÷200 MHz)	**crosstalk** < 0.2%
noise ≅ 1600 e^- @ C_D = 0; slope ≅ 80 e^-/pF	**propagation delay** 3.5 ns (3 fC ÷ 1 pC)
sensitivity ≅ 3.35 mV/fC ± 10%	**time walk** < 3.5 ns
BLR + discriminator offset < 0.13 fC (0.44 mV) r.m.s.	**output pulse width** 20÷200 ns (5% r.m.s. @ 50 ns)
max input signal before saturation ≅ 800 fC	**one shot dead time** 9 ns
input rate without loss of accuracy > 2 MHz @ 800 fC	**output t_r & t_f** < 2.5 ns

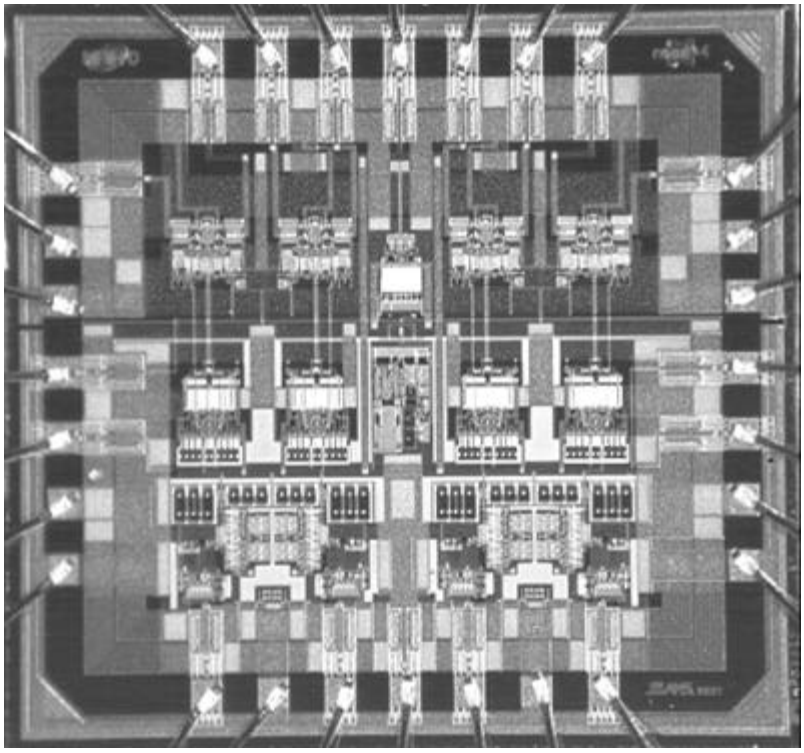

Figure 9: die photo (2.5 x 2.3 mm^2)