A PROTOTYPE FRONTEND ASIC FOR THE READOUT OF THE DRIFT TUBES OF CMS BARREL MUON DETECTOR

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DETECTOR PARAMETERS
&
FRONTEND DESIGN

- **Gas mixture $ArCO_2$ 85:15 @ atmospheric pressure**
- **Drift rate 55 μm/ns; max drift time 400 ns**
- **Low gain (50 K - 100 K) for long lifetime**
- **Maximum tube length 3 m; stainless steel wires $\phi = 50\mu m$**

➡ **Main goals are efficiency & time resolution**

The frontend task is to amplify signals, discriminate them against an external threshold and transmit the results to data acquisition. This must be accomplished in the smallest space and consuming very little power in order to maximize detector active volume and reduce service costs.

➡ Low noise, high gain analog chain.

➡ Fast rise time to minimize time walk due to different amplitude signals from drift tubes.

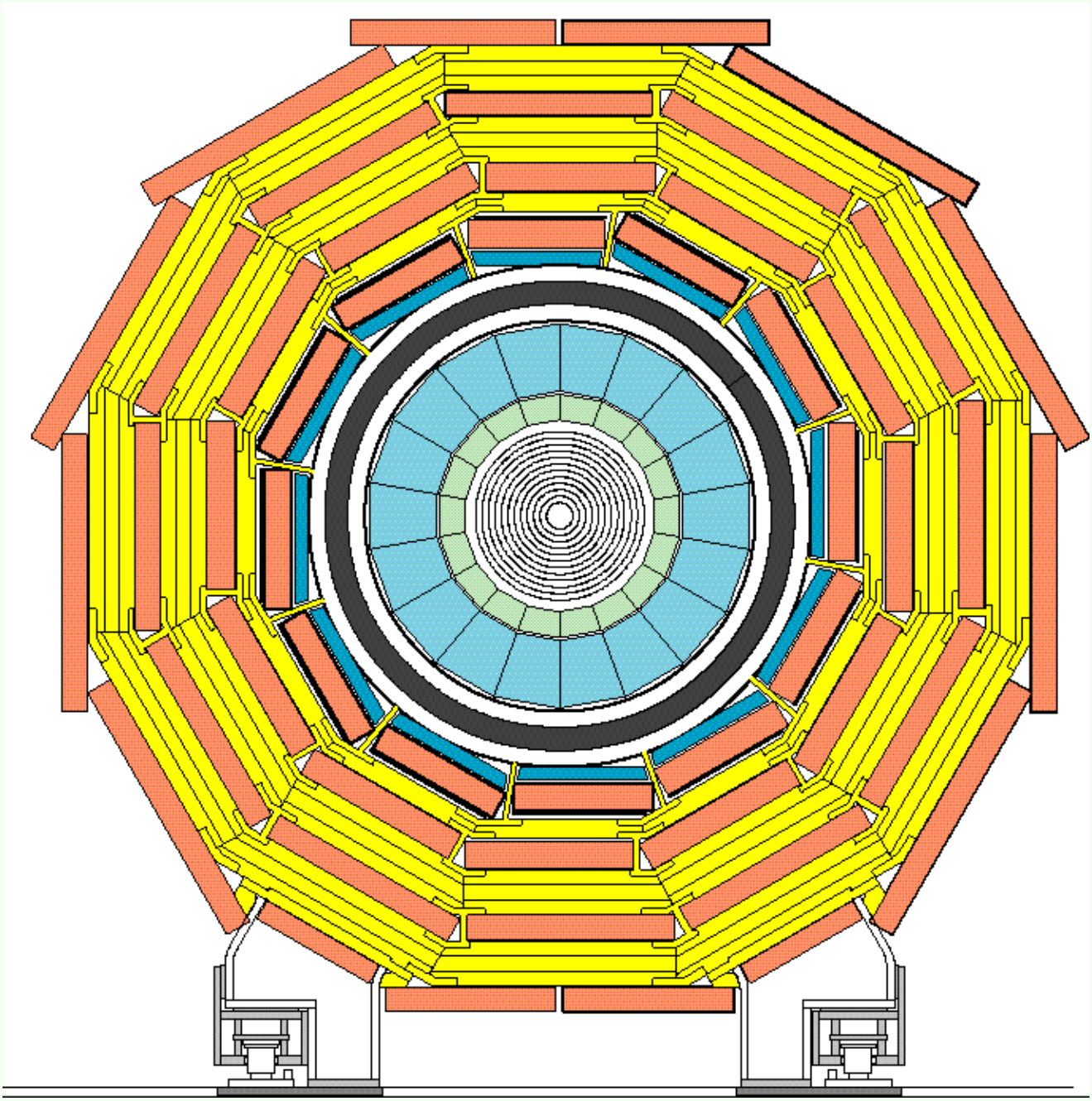
➡ Maximum uniformity among chips without equalization at wafer or board level. Hence low offsets and little tolerance for gain.

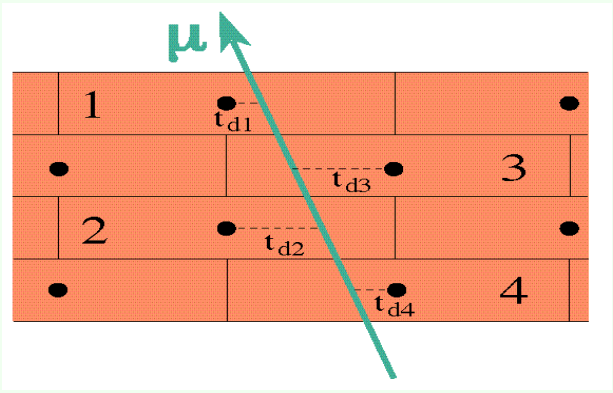
➡ Built in hysteresis to improve speed and stability.

➡ Programmable output width independent from signal amplitude to override cable bandwidth.

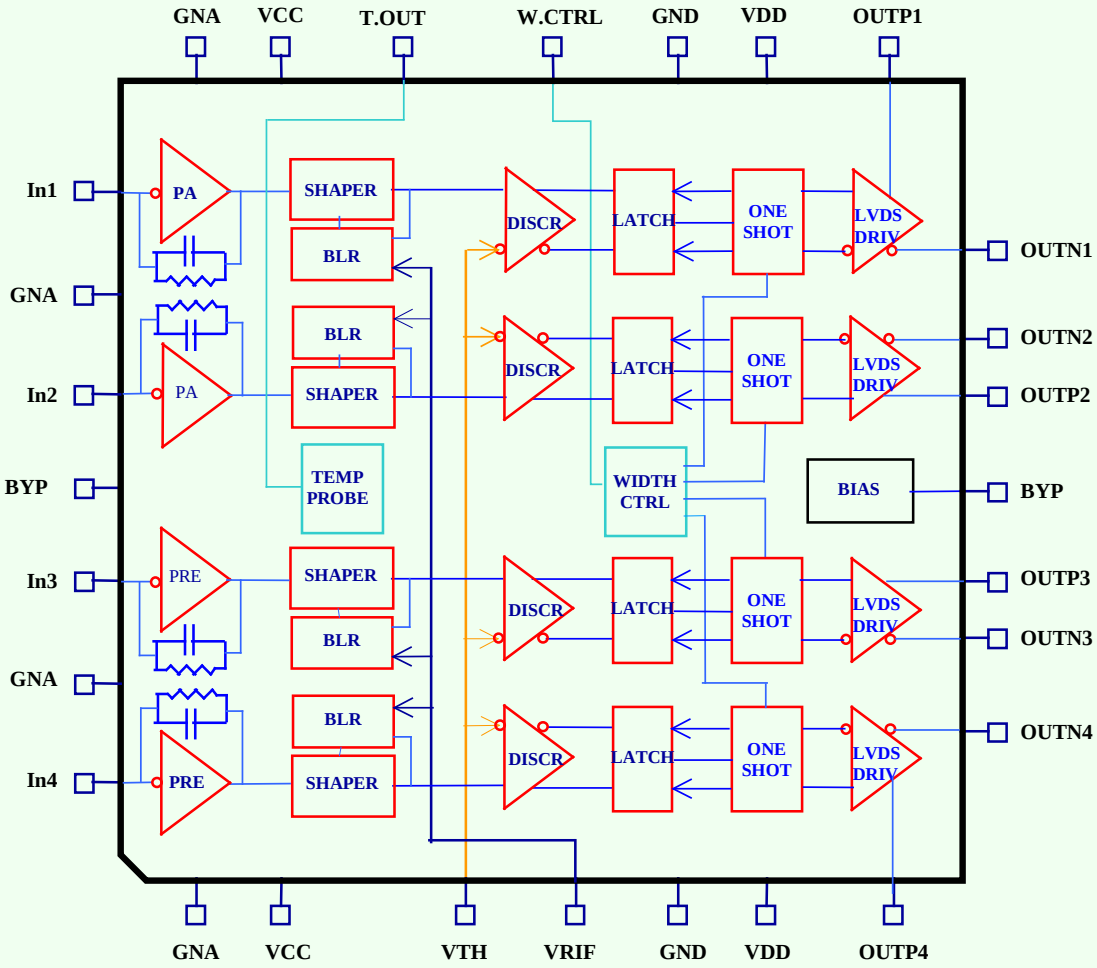
➡ Fast, low level (LVDS compatible) cable driver to minimize power and interferences.

➡ Other features for control & monitor purposes like the possibility of masking noisy channels and inclusion of a temperature sensor.




μ
1
2
3
4
t_{d1}
t_{d2}
t_{d3}
t_{d4}

CHIP UNDER TEST
block diagram

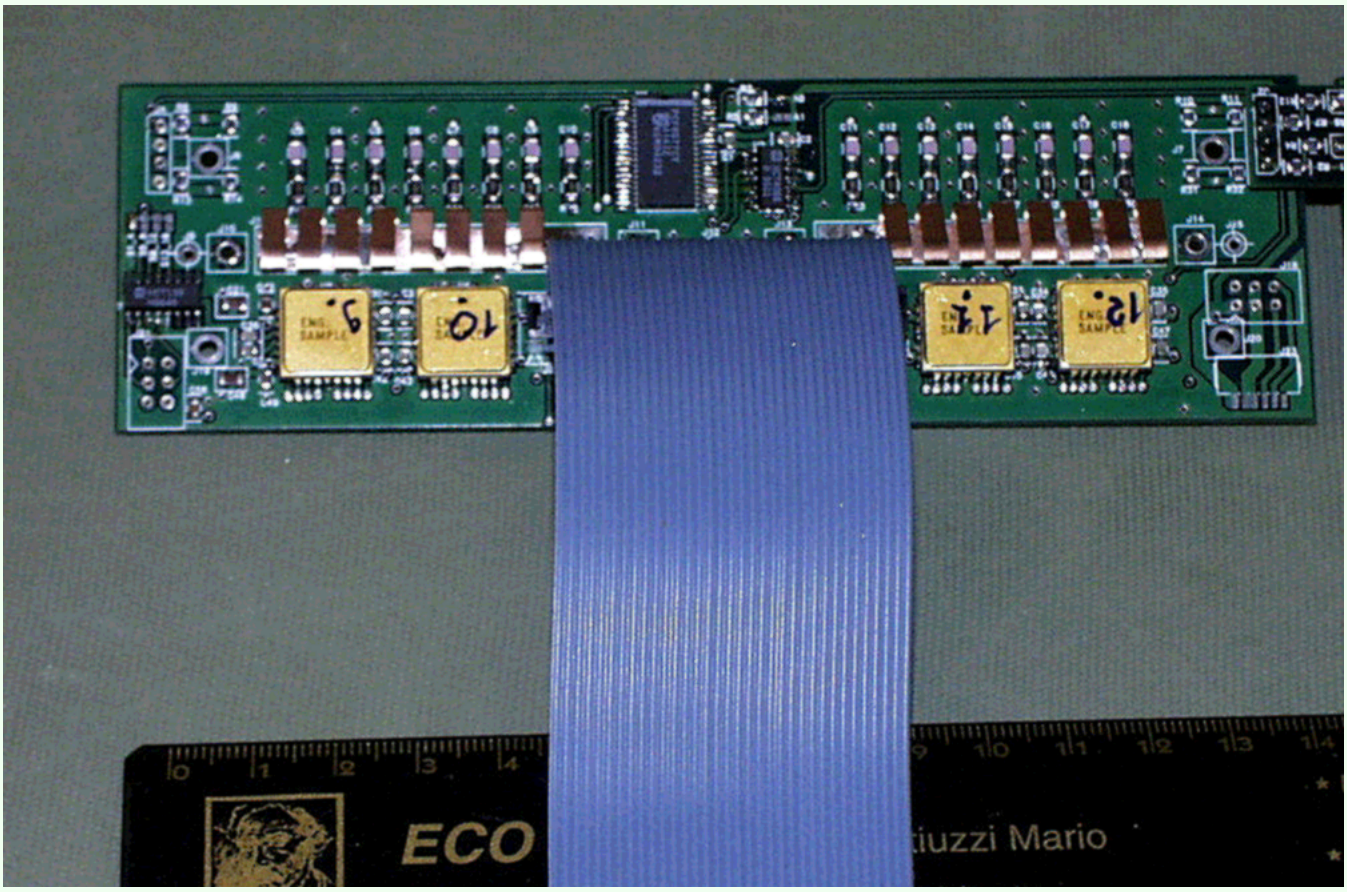


CHARACTERISTICS

- O.8 μm BiCMOS technology by AMS
- 4 channels in 2.5 x 2.3 mm^2 die area housed in 28 pin CLCC J-type case
- 2 MPW production runs for 110 untested samples; 96 fully working
- Preamplifier GBW > 1GHz (simulation) ; P ≅ 2.5 mW
- Simple shaper, with short integration time, inside feedback loop of a low offset OTA
- Baseline and threshold levels common to all channels
- One shot activated latch
- Voltage output cable driver with LVDS compatible levels; termination resistors inside pads
- temperature sensor output 7.5 mV/ ºK

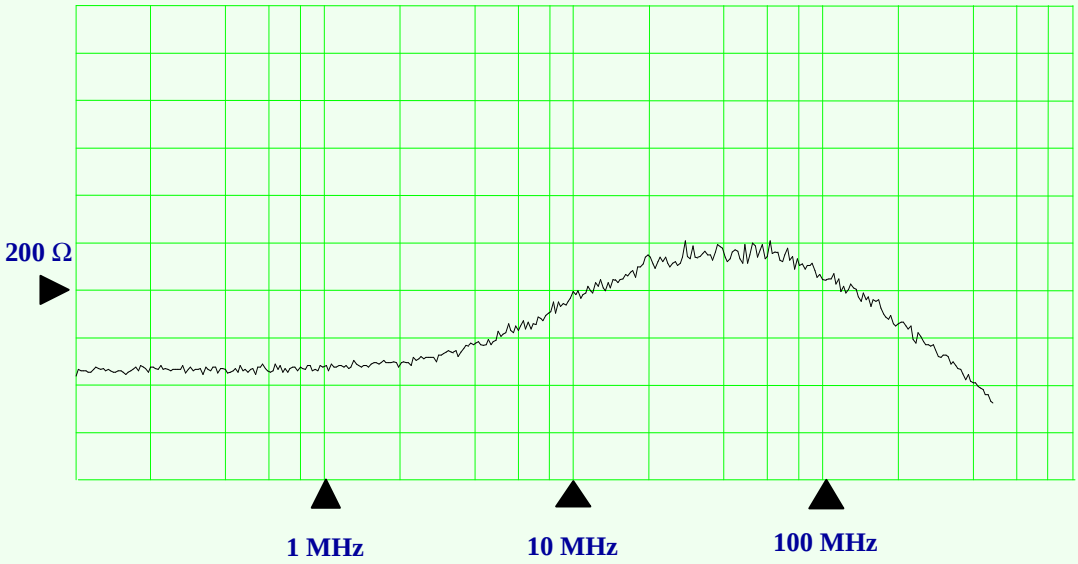
READOUT BOARD
using prototype ASICs

- 16 channels
- 155 x 45 mm^2 ; 4 layers
- I^2C interface for temperature readout & mask programming
  (last has been included to test interface needed for next ASIC)
- Double distribution of test pulse
- Additional protection diodes on inputs
- Total thickness (detector dead space) 25 mm
  (including input HV capacitor board)
- 1 superlayer of a typical chamber (56 chips) equipped Aug 98



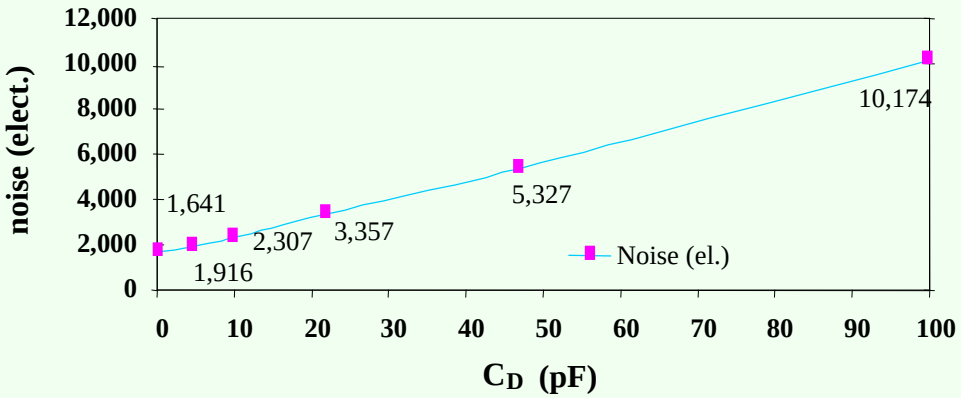
INPUT SECTION
Z_{in} & noise vs. C_D

Zin vs. frequency (100 KHz-1GHz; vertical scale 50Ω/div)



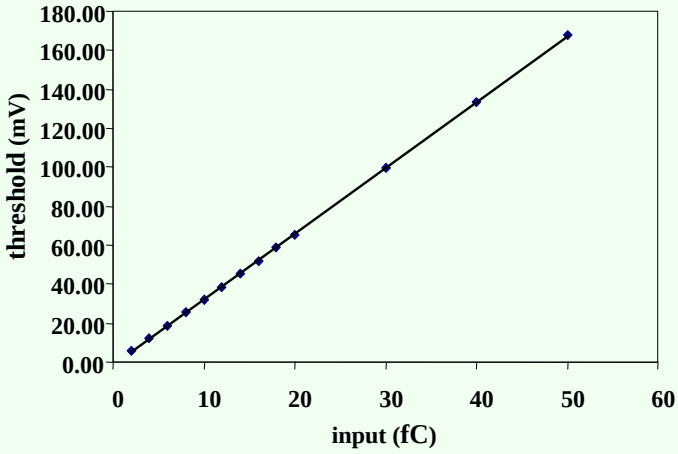
Stray capacitance lowers impedance value at high frequency

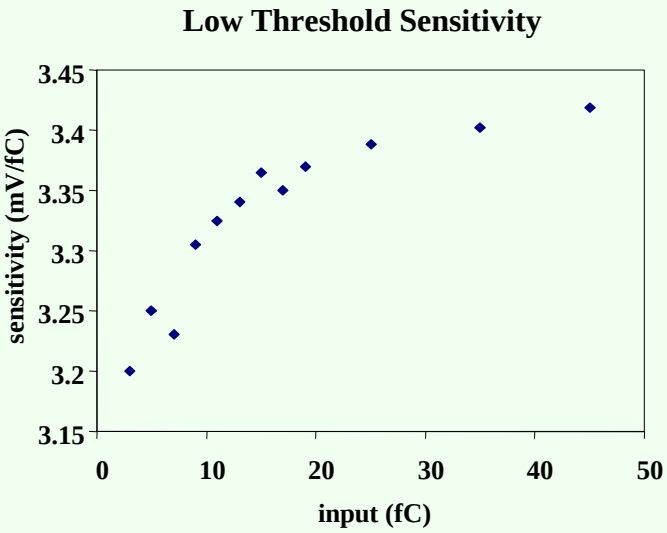
Noise vs. C_D



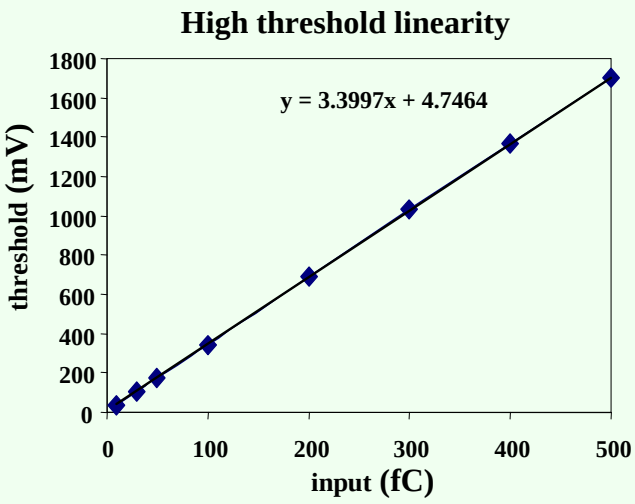
Slope 80e⁻/pF

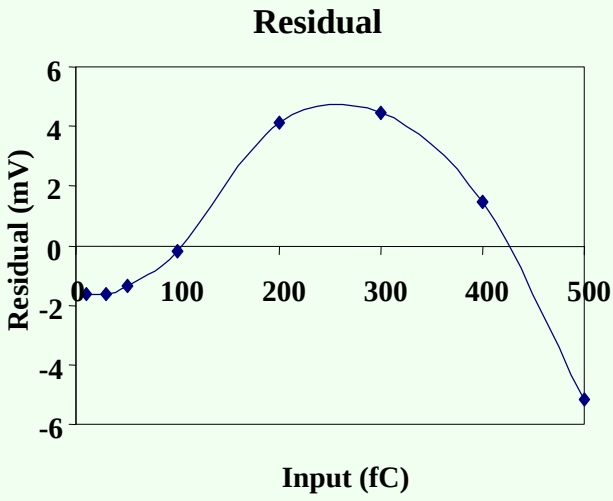
ANALOG SECTION
Sensitivity & Linearity





Loss of sensitivity at low input signals is probably effect of little dependence of discriminator behaviour on slew rate of input signal.

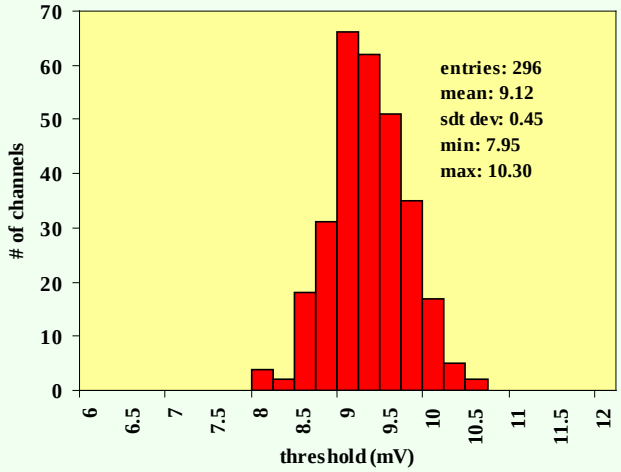




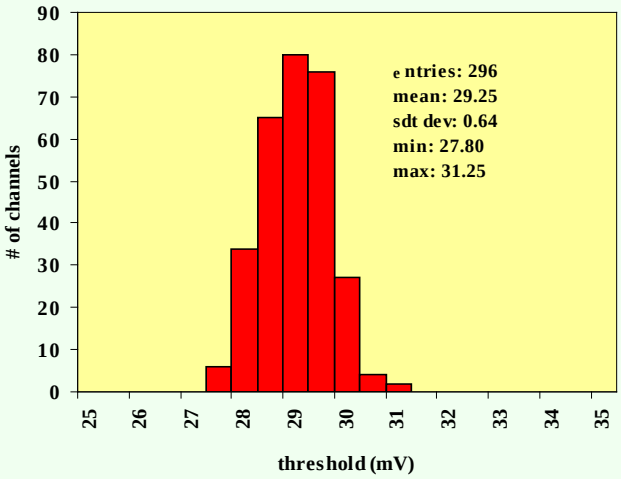
In this case slew rate limitation is the most probable cause of loss of linearity for high input signals. Error is anyhow within 1%.

CHIPS ON BOARD
threshold uniformity & noise

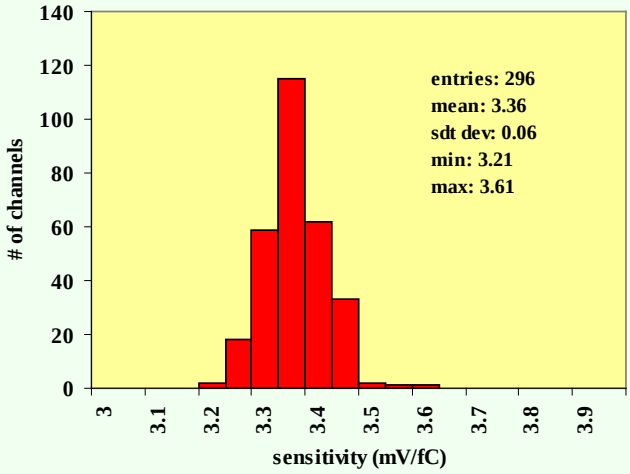
THRESHOLD @ 3 fC INPUT



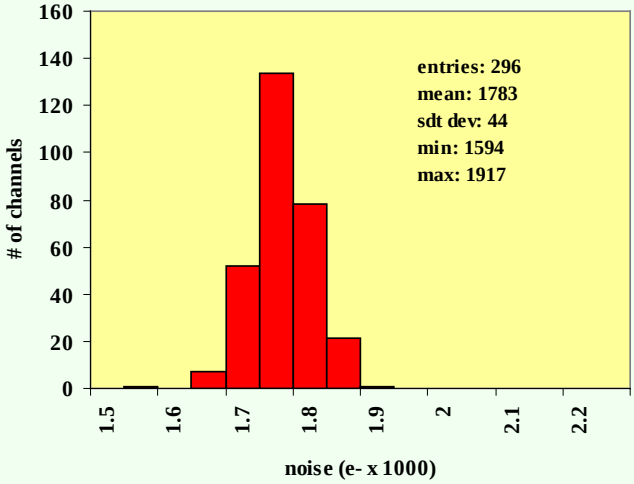
THRESHOLD @ 9 fC INPUT



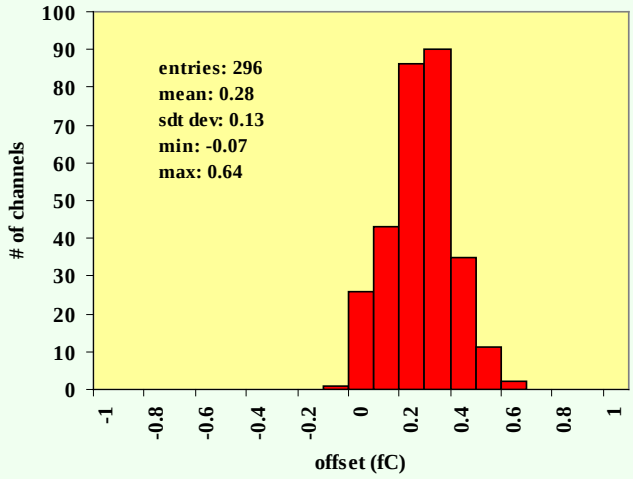
SENSITIVITY



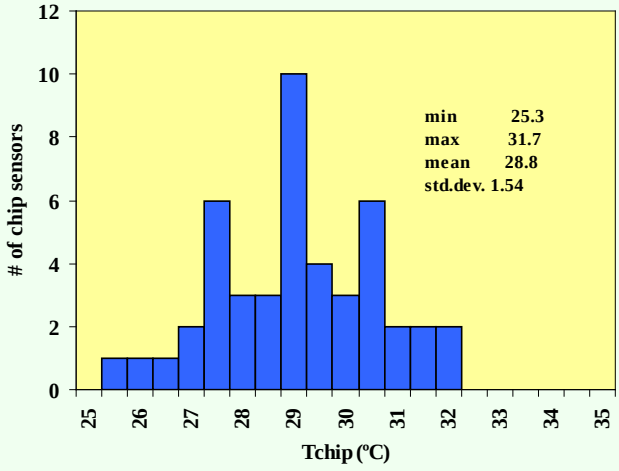
NOISE



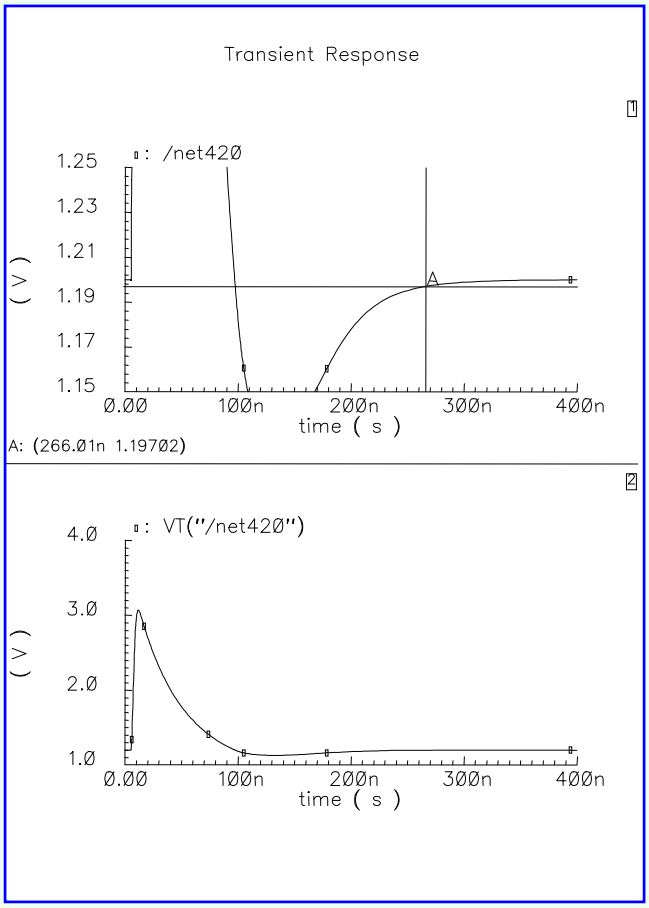
OFFSET FROM REGRESSION



TEMPERATURES INSIDE CHAMBER



ANALOG SECTION
max signal rate & crosstalk



This is a simulation plot.
Actually test was performed by injecting 1 pC pulses with a photodiode at rates up to 2 MHz and delayed 3 fC pulses using a capacitor.
Threshold was fixed to detect 50% of generator rate without light pulses.
There was no appreciable change in this percentage with light on and reducing the delay between light and charge pulses to less than 500 ns.

CROSSTALK

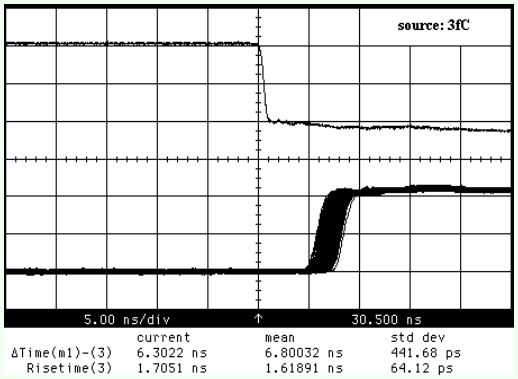
- **For each channel of one chip we measure the threshold level that makes it trigger at 50% of the rate at which neighbour channels are stimulated with charge pulses up to saturation.**
  Maximum threshold found is 0.2% of the sum of the pulses.
  Crosstalk reduces cutting PCB trace to input of channel under test.

- **Interference from output driver to analog section turned out to be at noise level even when an unterminated cable (worst condition) is connected.**

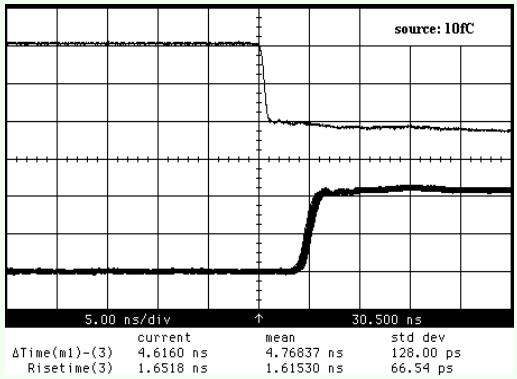
- **Crosstalk on readout board is 0.3% in average and includes contribution of test pulse distribution; it increases to a max 0.5% for the channel close to output flat cable.**

GENERAL TESTS
Time walk

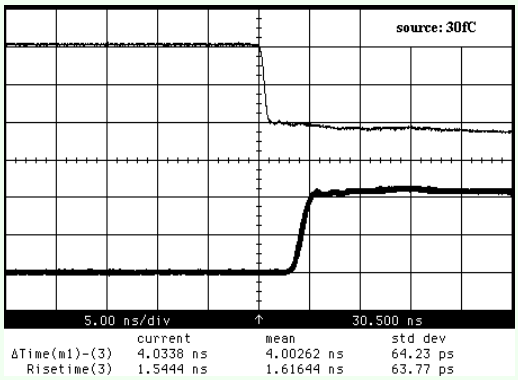
Fixed threshold : 1.5 fC. Different input charges



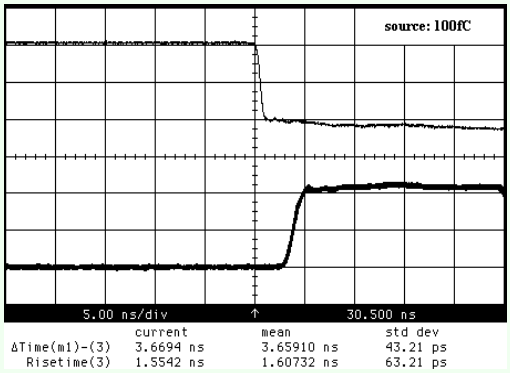
Input = 3 fC delay = 6.8 ns



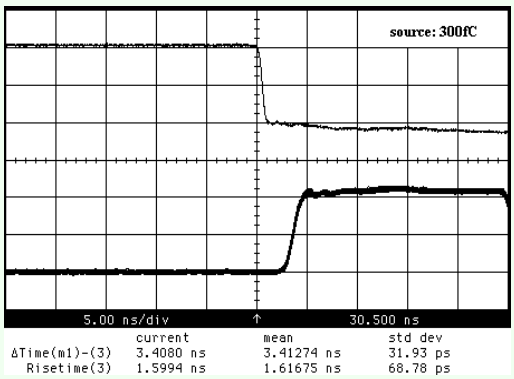
Input = 10 fC delay = 4.8 ns



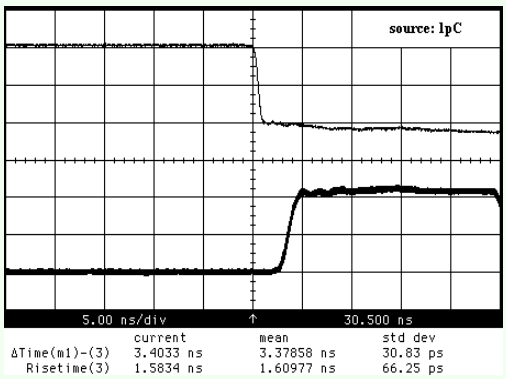
Input = 30 fC delay = 4.0 ns



Input = 100 fC delay = 3.7 ns

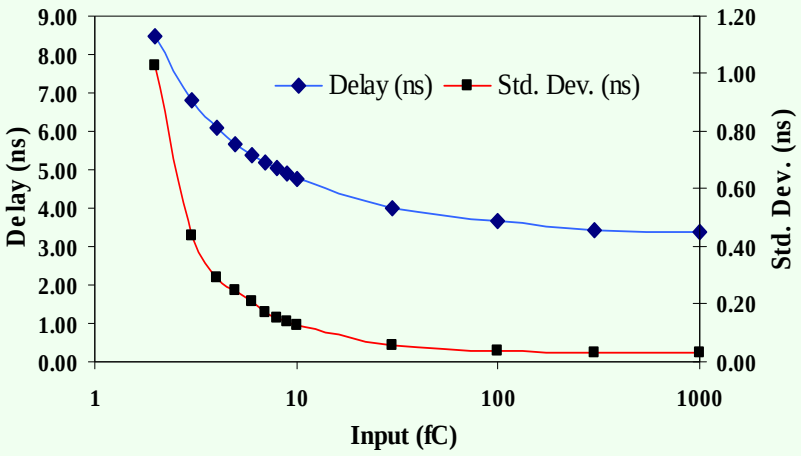


Input = 0.3 pC delay = 3.4 ns



Input = 1.0 pC delay = 3.4 ns

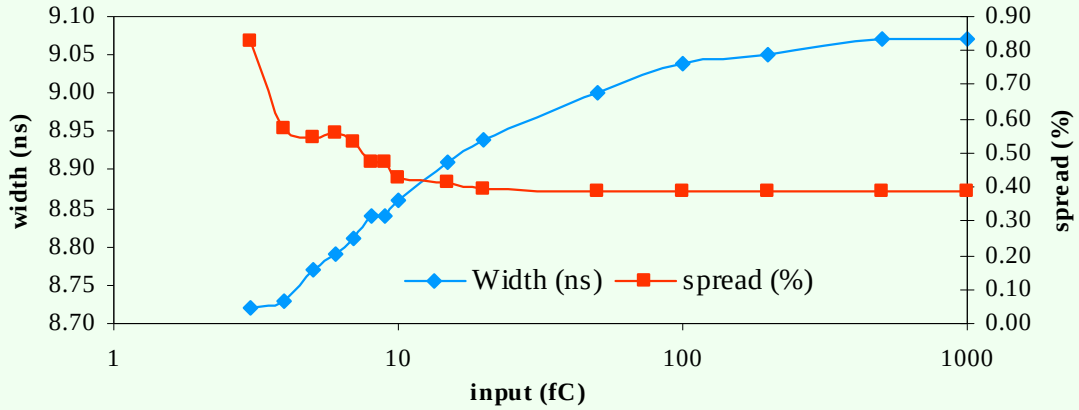
Time Walk (chip 8, ch 2)



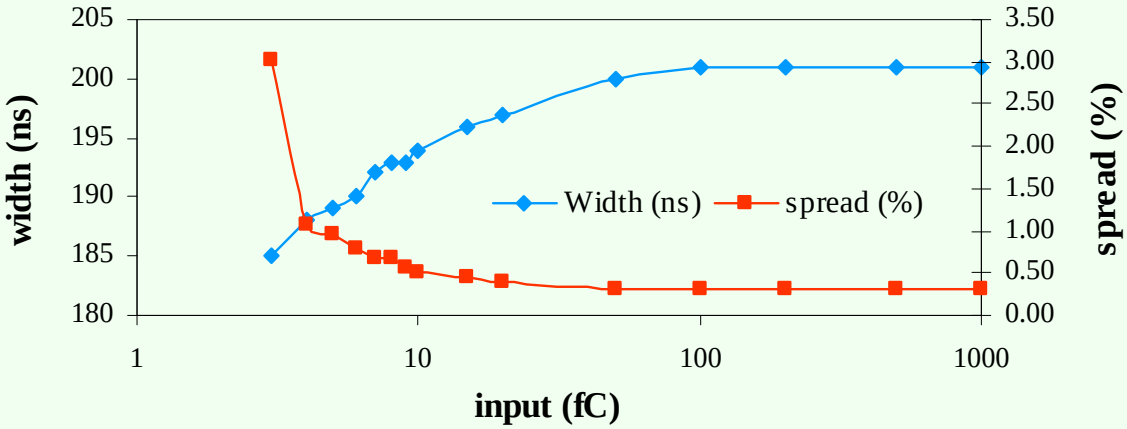
Plot of all data
pulser t_r = 0.7 ns
range 2 fC - 1 pC
rms due to noise

ONE SHOT WIDTH
max, min & dependence on signal

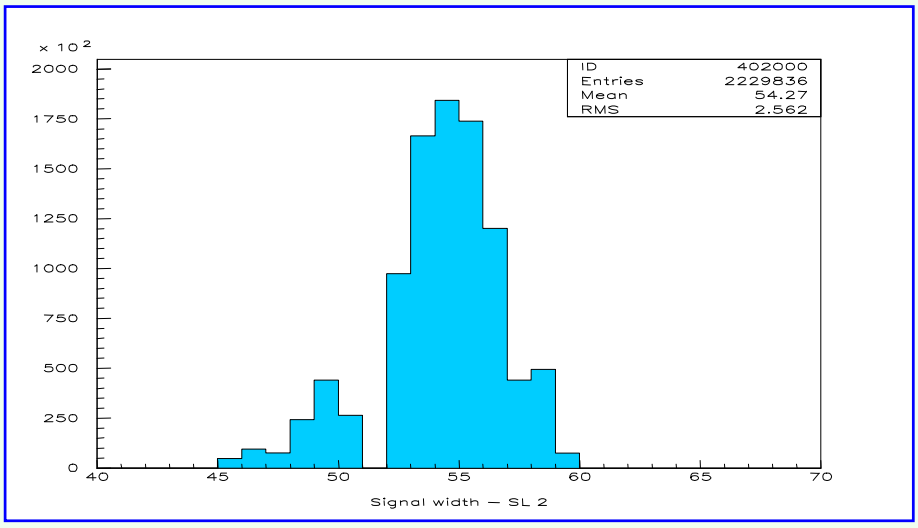
Min width



Max width

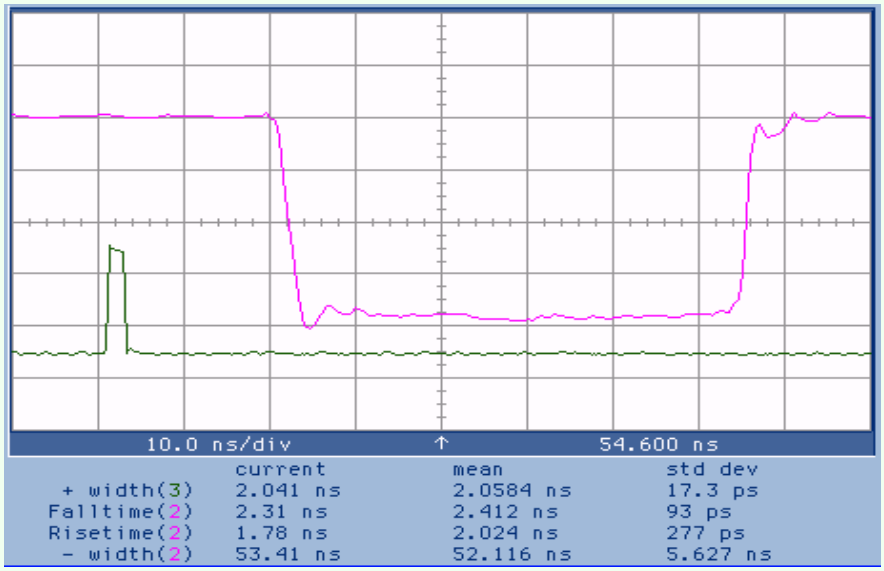


Spread of output pulse width



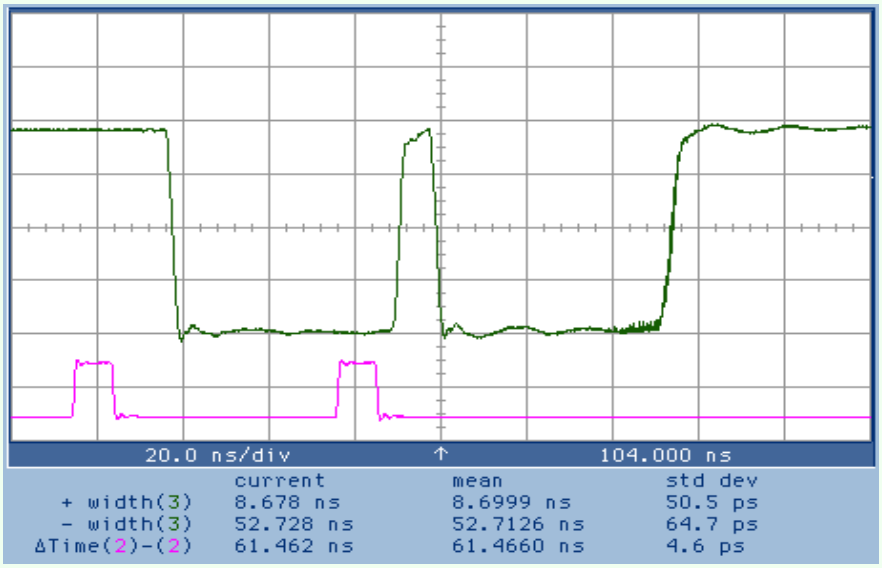
TIMING SIGNALS
discriminator, one shot &driver

Capture of narrow signals



Minimum width of dicriminator input signal: 2 ns pulses with 5 mV overdrive are captured with 99.9 % efficiency. Actual behaviour is better as for this test we use the output of the shaper (with its noise) as reference for comparator. Delay due to pulser trigger.

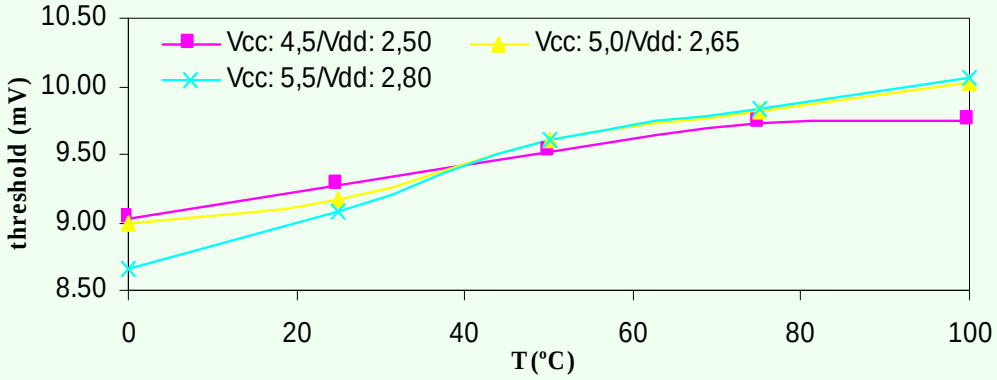
One shot dead time



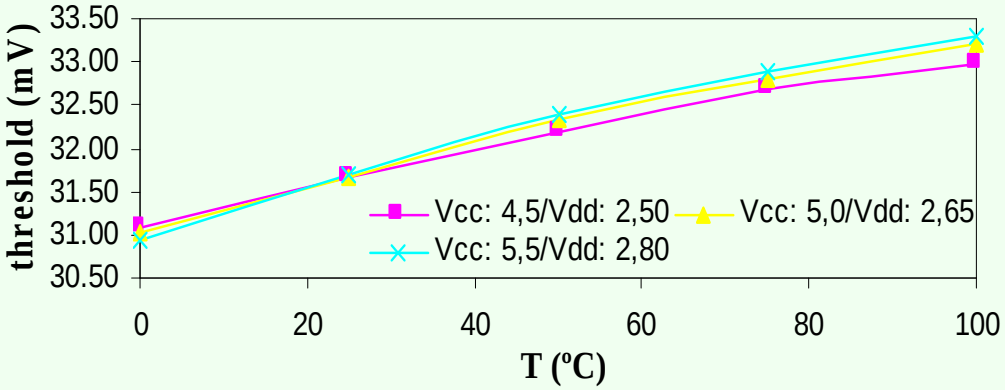
9 ns @ 50 ns pulse width; input output delay due to pulser trigger

DEPENDENCE ON TEMP. & SUPPLY
threshold, noise & sensitivity

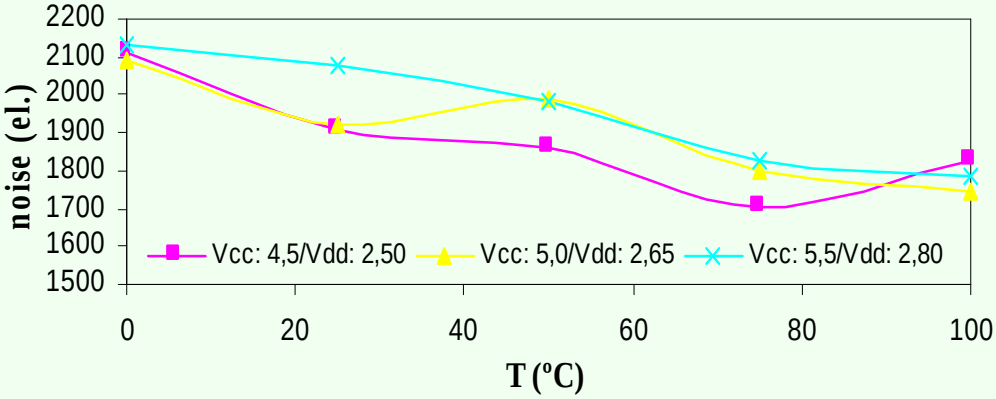
3fC threshold variation



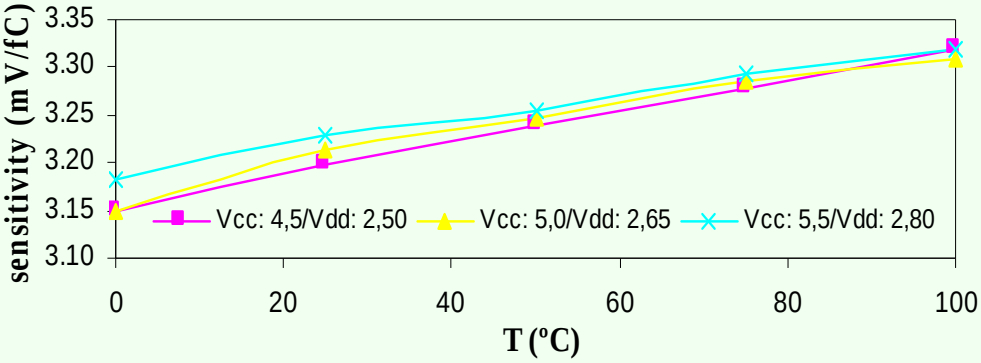
10fC threshold variation



noise

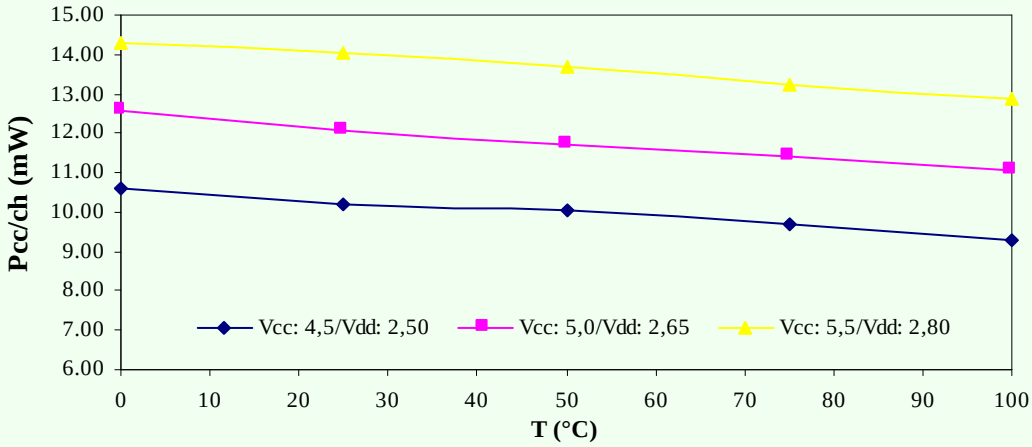


sensitivity

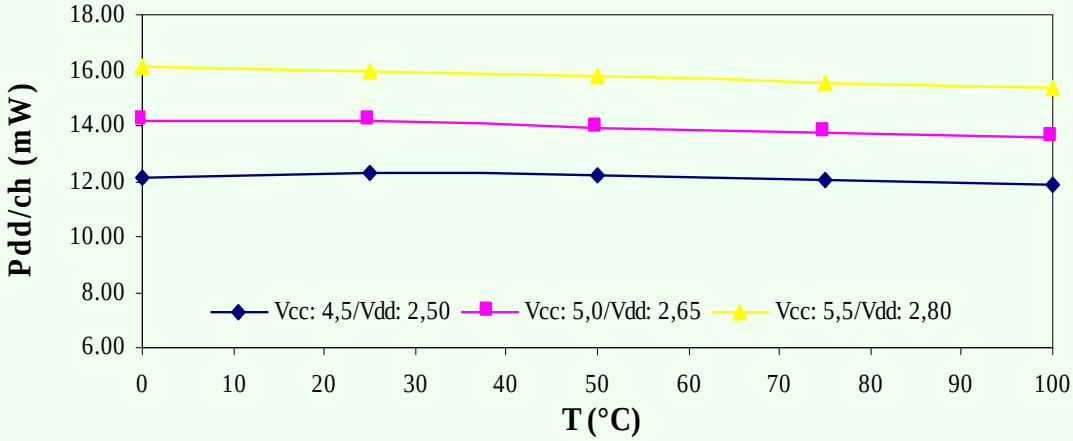


DEPENDENCE ON TEMP. & SUPPLY
power dissipation & output levels

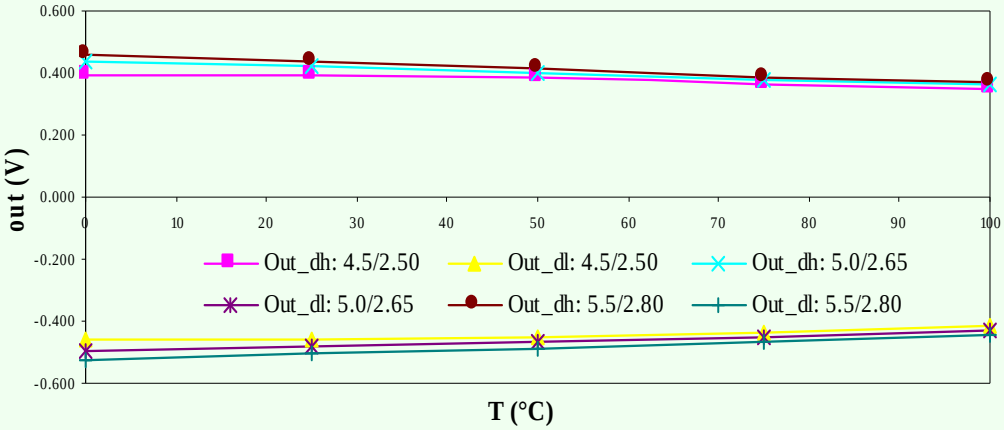
Pcc/channel



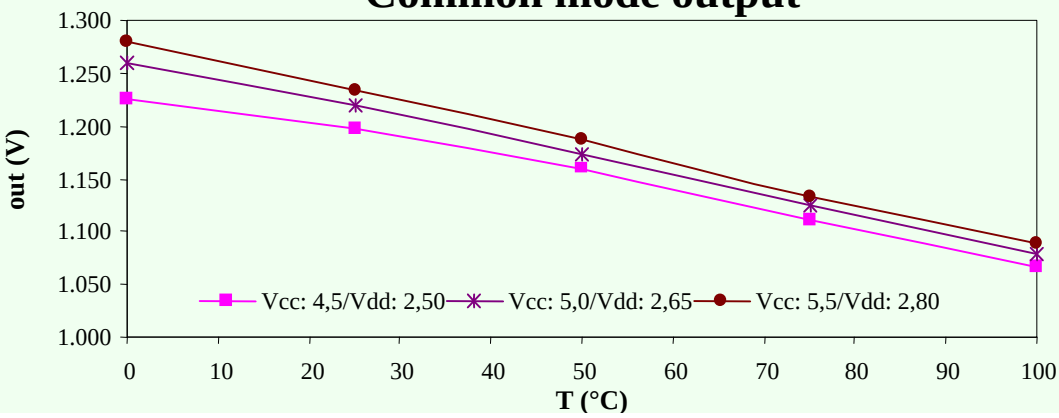
Pdd/channel



Differential output



Common mode output



PERFORMANCE SUMMARY

- **25 mW/ channel @ + 5 V& + 2.5 V (average of 56 chips) minimal variation with signal rate and temperature**
- **Zin ≅ 200 Ω** (5 MHz – 200 MHz)
- **noise ≅ 1600 e^- @ C_D = 0; slope ≅ 80 e^-/pF**
- **sensitivity ≅ 3.35 mV/fC ; capacitor tolerance (max 10%) affects uniformity for different batches**
- **baseline restorer + discriminator offset < 0.13 fC r.m.s.**
- **max input signal before saturation ≅ 800 fC**
- **threshold range 0 - 500 fC with < 1% nonlinearity**
- **max input rate without loss of accuracy > 2 MHz @ 1pC**
- **crosstalk < 0.2%**
- **propagation delay 3.5 ns ; time walk 3.5 ns (3fC - 1pC)**
- **output pulse width 20 - 200 ns (5% r.m.s. @ 50 ns) almost independent from signal amplitude**
- **one shot dead time 9 ns**
- **output t_r & t_f <** 2.5 **ns**
- **temperature sensor error 3 ^oK @ 25 ^oC**

STATUS - CONCLUSIONS

- **Very good performances at low power. Also yield seems good.**

- **4 different prototypes have been submitted to optimize circuits. One is now being tested for what concerns masking at shaper or discriminator stage and other features.**

- **Two runs used to equip a number statistically significant of drift tubes for test with muon beam. Analysis is in progress and preliminary results confirm bench tests.**

- **Improvements for next prototype :**

  Noise dependence on C_D is somewhat worse than simulated, need more current at input stage (1.5 mW).

  Different mask circuit as current one has some feedthrough using fast control signals.

- **Further work need to be carried out on following items:**

  Radiation tolerance to neutrons (γ already tested).

  Protection to ESD.

  MTBF.

  Definition of test at wafer level.

- **We plan to have another prototype run by the end of year in order to test the finalized design.**

  This design should include all modifications (modified masks etc.) and be packaged in QFP 44 case.